

# Using Stochastic Computing to Reduce the Hardware Requirements for a Restricted Boltzmann Machine Classifier

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# Overview

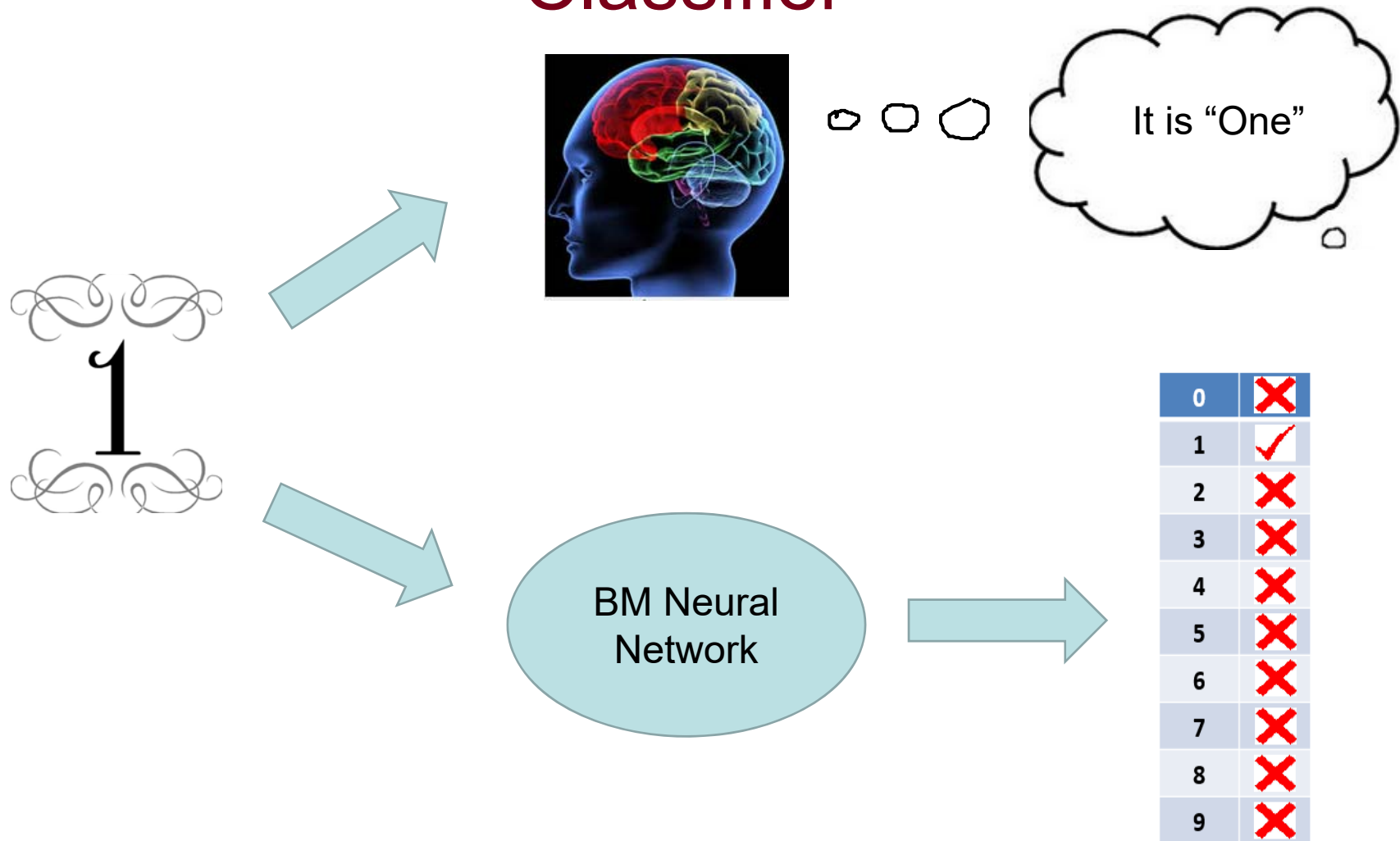
- Restricted Boltzmann Machine classifier
- Stochastic computing
- Results



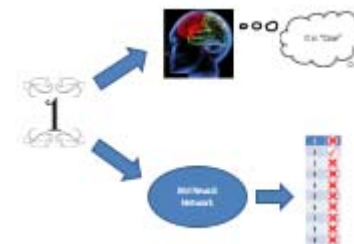
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# Restricted Boltzmann Machine Classifier



# BM Structure



**Input:**  
28 x 28 = 784 pixels

*Weight*

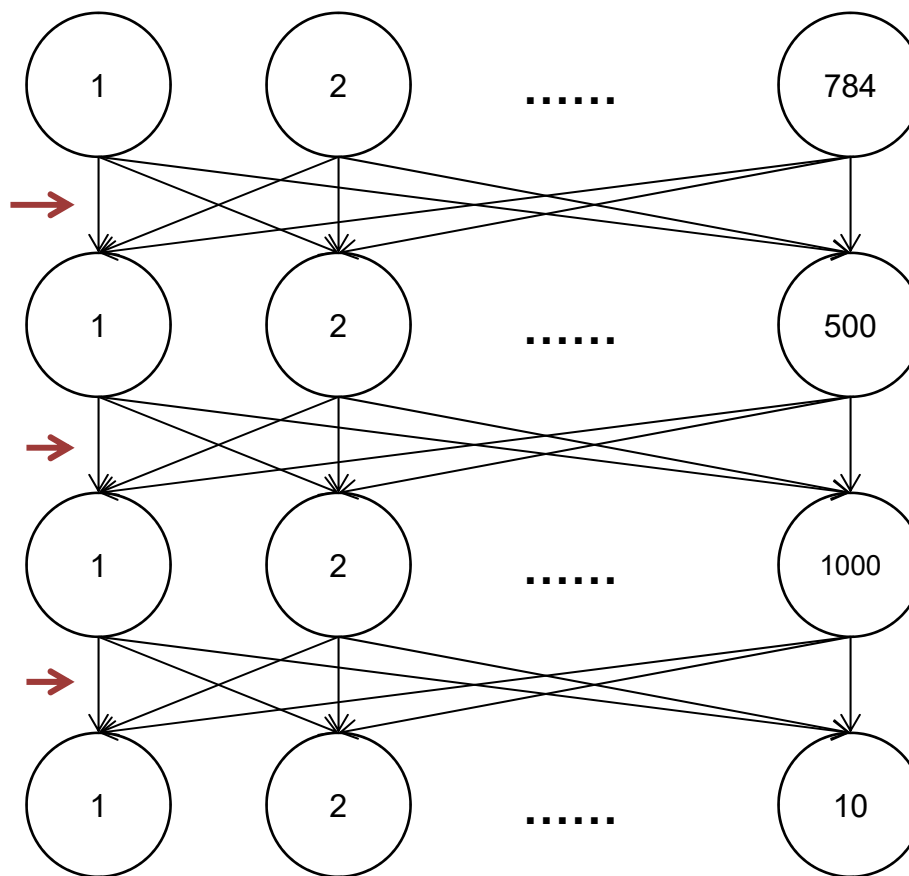
1<sup>st</sup> Hidden Layer

*Weight*

2<sup>nd</sup> Hidden Layer

*Weight*

**Outputs:**  
ten labels from 0 to 9.



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# Stochastic computing

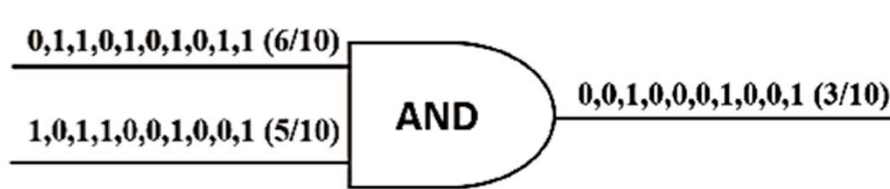


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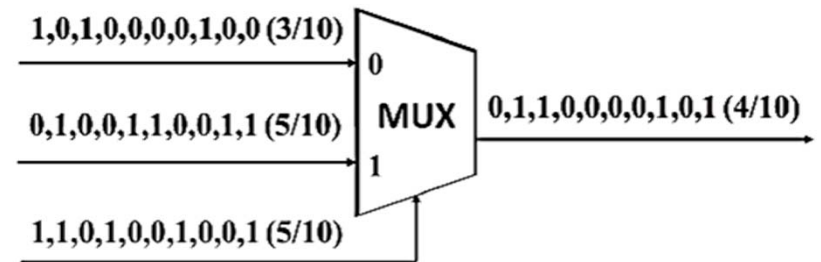
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# Background: Stochastic Computation

- Complex operations can be performed with very simple logic.



**An example of multiplication  
using an AND gate**



**An example of scaled addition  
using a MUX unit**

A reduction in area of 50x or 100x compared to conventional implementations is common.



# Stochastic computation components

- Sigmoid function,  $\text{Tanh}(x)$
- Matrix multiplication: Uni-pos-neg adder
- Unipolar/Bipolar multiplication
- Unipolar/Bipolar addition



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# Results: Error rate and speed

Table I. Error rate comparison

Sizes	Conventional	Stochastic			
		512	1024	2048	4096
100 × 200 × 10	1.96%	10.06%	5.72%	3.91%	3.14%
200 × 400 × 10	1.35%	7.93%	4.24%	3.08%	2.35%
300 × 600 × 10	1.17%	6.33%	2.92%	1.80%	1.80%
400 × 800 × 10	1.10%	4.17%	2.37%	1.52%	1.34%
500 × 1000 × 10	0.98%	5.10%	2.32%	1.64%	1.32%

Table II. Speed comparison

Size	CPU(s)	FPGA(s)	Speedup
100 × 200 × 10	$6.2 \times 10^{-3}$	$8.561 \times 10^{-6}$	724.2
200 × 400 × 10	$7.8 \times 10^{-3}$	$9.682 \times 10^{-6}$	805.6
300 × 600 × 10	$9.2 \times 10^{-3}$	$9.797 \times 10^{-6}$	939.1
400 × 800 × 10	$1.32 \times 10^{-2}$	$1.025 \times 10^{-5}$	1287.8
500 × 1000 × 10	$1.66 \times 10^{-2}$	$1.077 \times 10^{-5}$	1541.3





# Result: Fault tolerance

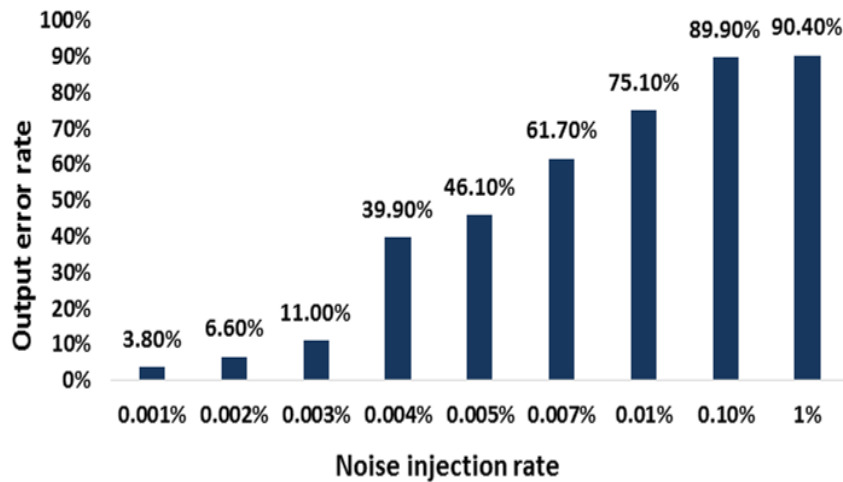


Figure 1: Output error rates obtained from injecting different rates of faults into the conventional architecture

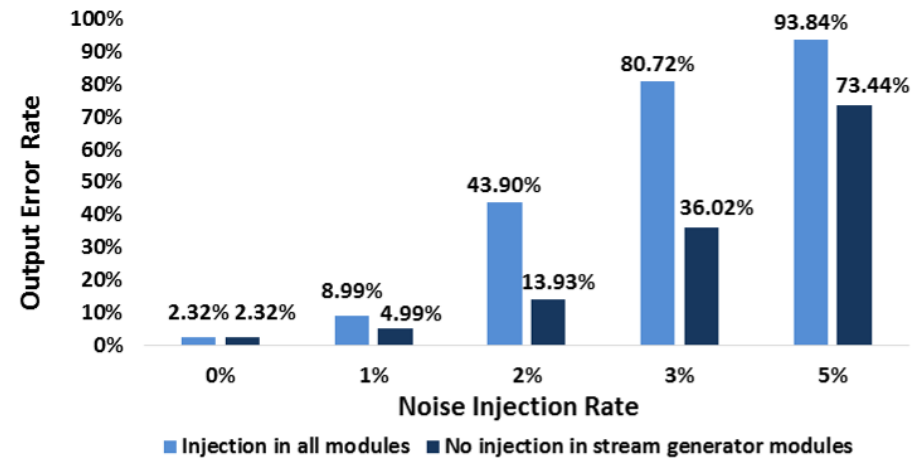


Figure 2: Output error rates obtained from injecting different rates of faults into the stochastic architecture

- Stochastic architecture to gracefully tolerate about a 1%-2% fault rate in its internal computing circuits.



Thanks!  
Q&A: please go to my poster  
section



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