

Pitfalls & Trade-offs in Simultaneous, On-Chip FPGA Delay Measurement

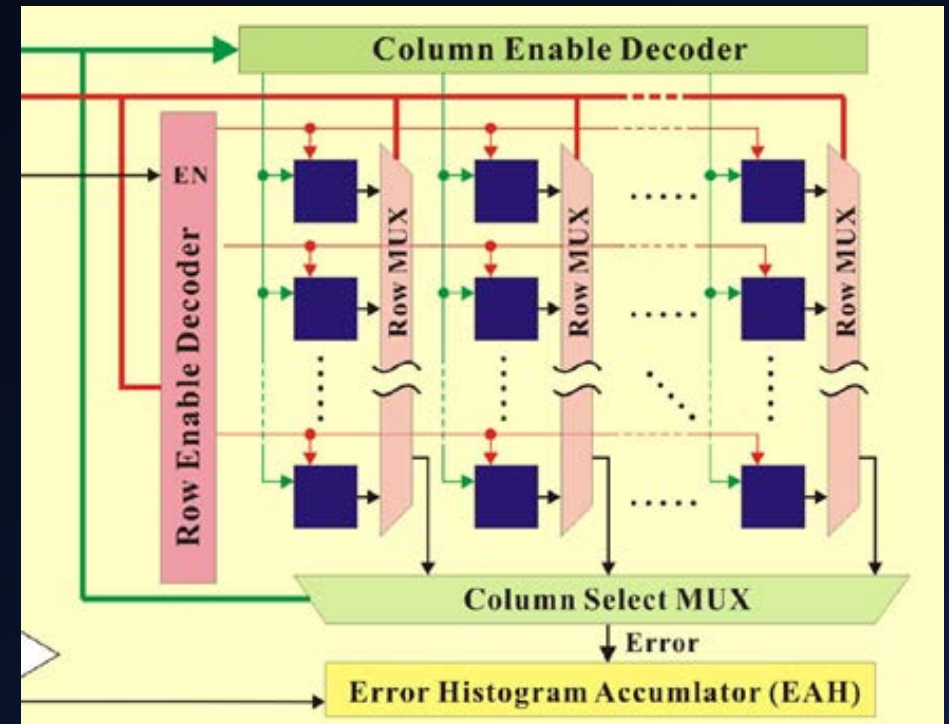
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FPGA 2016

FPGA Self-Measurement

- Map component delays
- Previous FPGA measurement work
 - Imperial, 2009
 - Penn, 2014
- Is parallel measurement accurate?

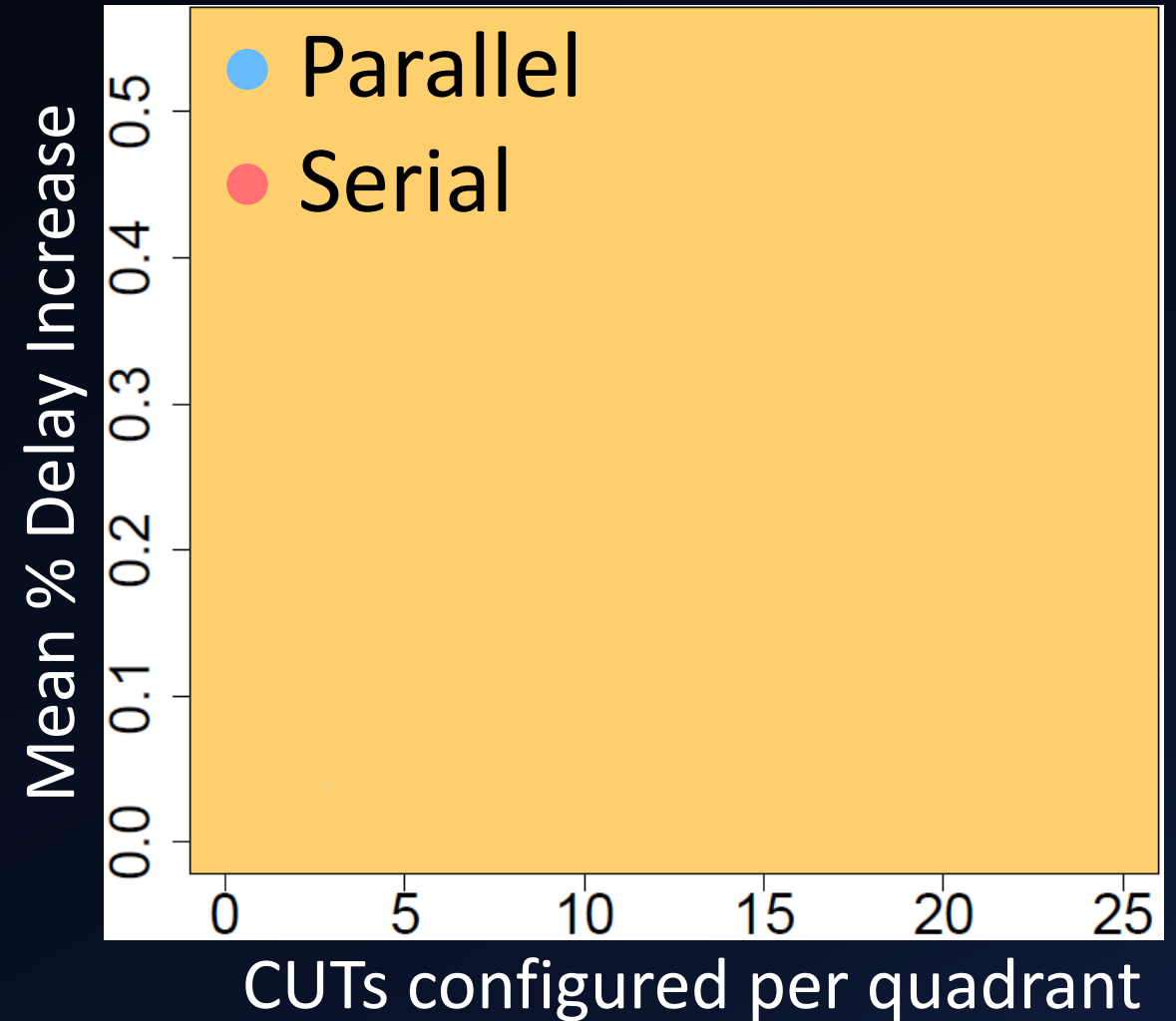
	End LE															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		422	414	415	407	418	423	435	431	416	428	427	422	433	412	414
2	398		400	412	393	409	412	417	420	404	414	411	406	412	395	397
3	385	398		389	376	387	395	404	401	387	398	400	390	401	381	384
4	398	399	393		379	391	400	403	401	384	398	403	398	404	384	395
5	393	404	396	397		393	401	412	411	392	406	406	400	411	389	393
6	398	404	395	390	378		401	404	404	388	401	401	398	408	381	395
7	393	397	390	382	376	385		400	396	379	393	395	390	400	376	387
8	381	390	381	382	371	378	384		389	375	387	389	382	393	371	376
9	382	387	381	381	370	379	387	395		374	383	386	378	390	370	375
10	395	402	395	397	384	391	399	409	402		399	400	393	404	381	387
11	392	401	392	393	381	390	398	406	401	383		398	390	398	379	382
12	395	401	392	389	376	390	398	398	398	379	393		382	398	370	389
13	395	403	395	395	382	393	401	411	400	386	401	397		398	377	382
14	395	400	392	387	378	390	398	398	395	378	392	393	381		368	385
15	397	405	393	397	382	395	400	411	401	389	398	400	385	401		384
16	411	414	406	403	390	404	409	414	409	392	409	407	393	411	384	

LUT-to-LUT delays



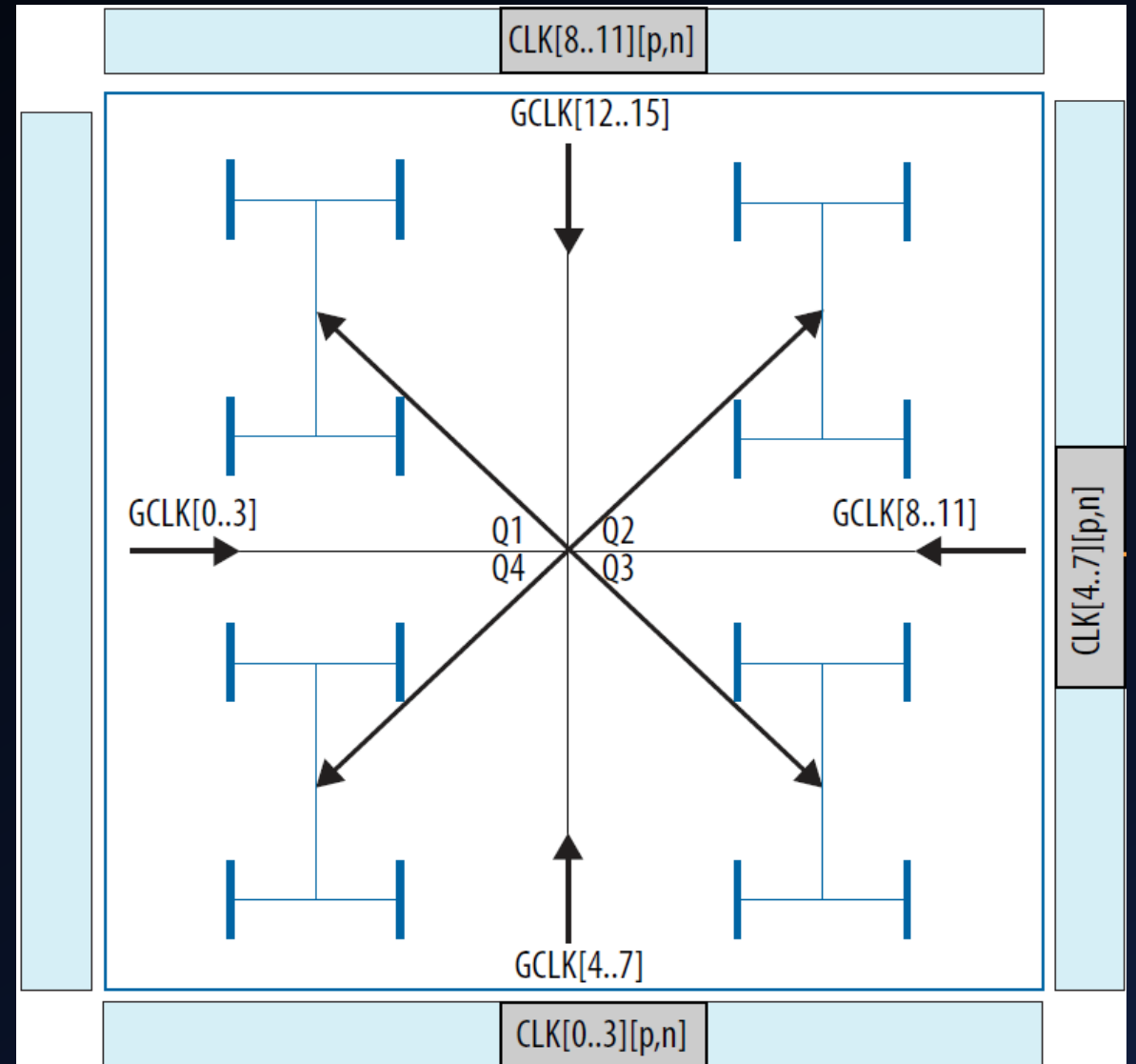
Parallelism Affects Results

- Activating logic increases delays
- Instantiating logic increases measured delays



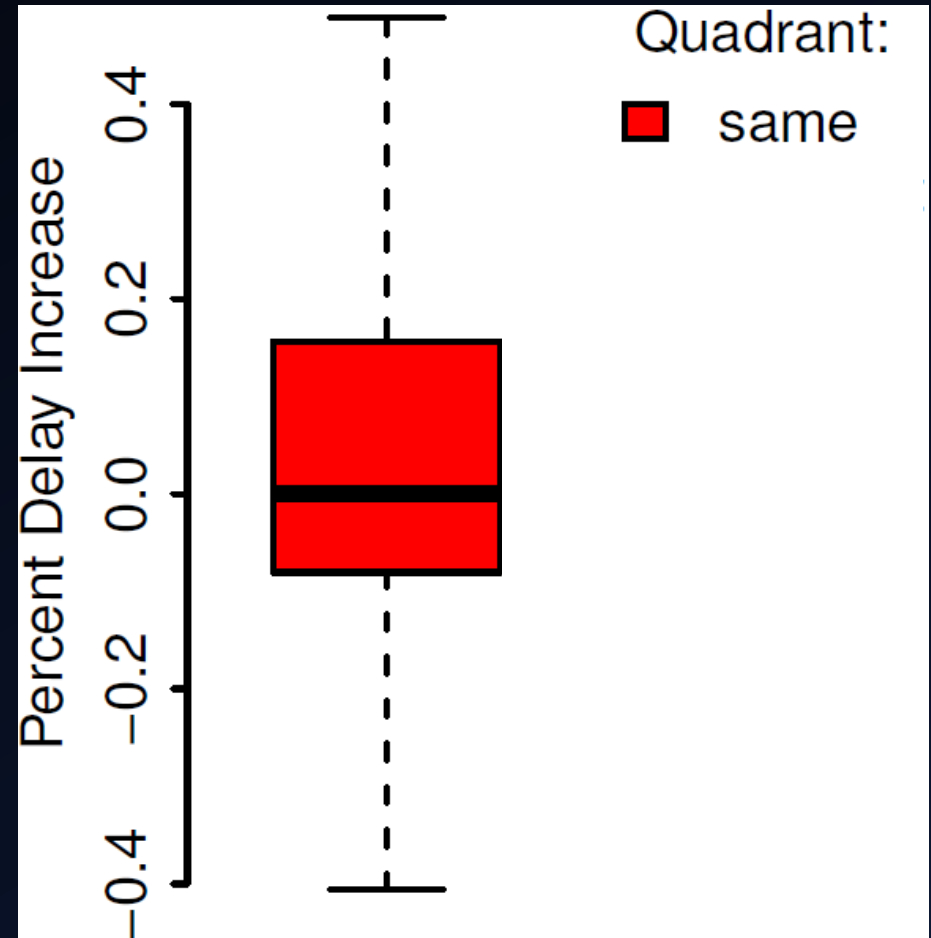
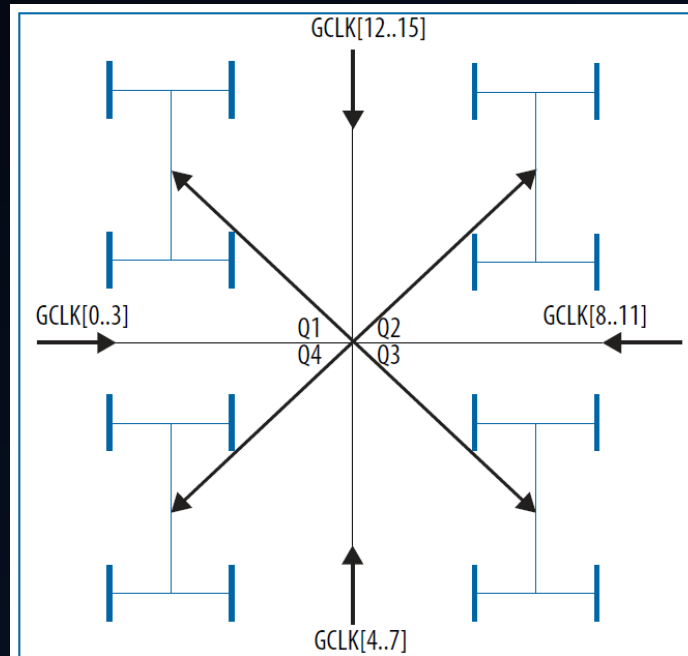
What's Happening?

- Self-heating
- Voltage loading
- Increased clock activity
 - Placement of circuits activates additional clocks



Relative Location Affects Results

- Parallel measurement in same quadrants increases variation
- Use of different quadrants mitigates error



Conclusions

- Parallel measurement possible with increased error
- Inactive logic increases error
- Informed placement of logic improves accuracy

