Call for Papers: FPGA 2020

Twenty-Eighth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays
http://www.isfpga.org

February 23-25, 2020
Embassy Suites by Hilton Monterey Bay Seaside
1441 Canyon Del Rey, Seaside, California, 93955, USA

Abstract Submission Deadline:	~~September 9, 2019~~ September 10, 2019
Full paper Submission Deadline:	~~September 9, 2019~~ September 16, 2019
NEW Artifact Submission Deadline:	~~September 9, 2019~~ September 16, 2019

Submission website is open

Artifact description and evaluation guideline is online

The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2020) is the premier conference for presentation of advances in FPGA technology. Accepted papers will be published in the conference proceedings and available in the ACM Digital Library.

Types of Submissions Sought

1. Research Papers (with and without Artifacts)

As usual, we solicit research papers related to the following areas:

- FPGA Architecture: Architectures for programmable logic fabrics or their components, including routing, flexible logic cells, embedded blocks (memory, DSP, processors), and I/O interfaces. Novel commercial architectures and architectural features.
- FPGA Circuit Design: Circuits and layout techniques for the design of FPGAs. Impact of future process and design technologies on FPGAs as well as novel memory memory or nano-scale devices. Methods for analyzing and improving static and dynamic power, power and clock distribution, yield, manufacturability, security, reliability, and testability.
- CAD for FPGAs: Algorithms for synthesis, technology mapping, logic and timing optimization, clustering, placement, and routing of FPGAs. Novel design software for system-level partitioning, debug, and verification. Algorithms for modeling, analysis and optimization of timing and power.
- High-Level Abstractions and Tools for FPGAs: General-purpose and domain-specific languages, tools, and techniques to facilitate the design, debugging and verification of FPGA-based applications and systems. Novel hardware/software co-design and high-level synthesis methodologies enabling digital signal processing, compute acceleration, networking, machine learning, and embedded systems.

- FPGA-based and FPGA-like Computing Engines: Systems and software for compiled accelerators, reconfigurable/adaptive computing, and rapid-prototyping. Programmable overlay architectures implemented using FPGAs.
- Applications and Design Studies: Implementation of novel designs on FPGAs establishing state-of-the-art in high-performance, low-power, security, or high-reliability. Designs leveraging unique capabilities of FPGA architectures or demonstrating significant improvements over alternative programmable technologies (e.g., CPU, GPU). Design studies or architecture explorations enabling improvement of FPGA architectures.

Research submissions may be either:

- Full: at most 10 pages (excluding references), for a full presentation at the conference; or
- Short: at most 6 pages (excluding references), for a brief presentation.

A paper submitted as either full or short will only be considered in that category and may include artifacts if desired (see below for more details on artifact submission and evaluation).

2. Tutorial Papers on Emerging Applications / Methodologies

The conference will include a Sunday workshop oriented toward users of FPGAs: be it deep learning implementations, computer security or other emerging topics of interest. For this category, we solicit tutorial papers describing effective design techniques and design flows. The ideal submission will enable beginning researchers to enter the area, current researchers to broaden their scope, and practitioners to gain new insights and applicable skills. Tutorial submissions need not present novel research results, but should integrate expert practical and/or research knowledge related to FPGAs for a broader audience. This may include:

- Technical descriptions of new commercial or academic design tools of general interest;
- Insightful summaries of the state-of-the-art that suggest open research problems; and
- In-depth design tutorials and design experiences.

Tutorial submissions are at least 4 and at most 10 pages. Accepted submissions are published in the proceedings and allocated a presentation time of up to one hour, appropriate to the content.

3. Panel Discussion Proposals

We also solicit proposals for the panel discussion at the conference banquet. The submission should outline the topic, questions to be addressed, and suggested speakers.

Submission Process - please read carefully

Submissions of all types should be made in the form of an English language PDF file, on-line at https://www.softconf.com/j/fpga2020/. Papers should use the sigconf ACM format template posted at http://www.acm.org/publications/proceedings-template/. LaTeX users should use the format used in the "sample-sigconf.pdf" file under the "Samples" folder of the zipped master file (downloadable through the "LaTeX (Version 1.61)" link). Microsoft Word users can download the file "**Interim layout.docx**" under the "Word Authors" section of the page. Abstract, Full Paper, and Artifacts Submissions must be received by **September 10, September 16, and September 16, 2019 at 11:59 PM AoE** (Anywhere-on-Earth time zone), respectively.

Submissions will be considered for acceptance as full or short regular papers, workshop papers, or posters. Regular submissions related to the workshop topic may be scheduled for presentation during the workshop. Regular or workshop submissions will also be considered for acceptance as a poster. A paper submitted to the short or full paper category will only be considered in that category. Once a paper has been submitted, its authorship list is considered to be fixed and finalized. As the inclusion and evaluation of artifacts is new for FPGA 2020, additional information is available at http://www.isfpga.org/artifactEvaluation.html.

Double Blind Policy:

The FPGA Symposium uses a double-blind reviewing system. **Manuscripts must not identify authors or their affiliations; those that do will not be considered.** References to the authors' prior work should be made in the 3rd person, in the same way one would reference work by others. If necessary to maintain anonymity, citations may be shown as "Removed for blind review," but consider that this may impede a thorough review if the removed citation is crucial to understanding the submission. When necessary, authors should cite widely-available Open Source software website(s) without claiming ownership. Grant numbers and other government markings should also be blinded during the review process. Placing a preliminary version of the unpublished paper on arXiv is not disqualifying, but it is also not encouraged. Similarly, if a paper can be unblinded by active search, this is not considered to undermine the spirit of the double-blind review. However, there are resources to blind open-source repositories for review, including: https://github.com/tdurieux/anonymous_github.) ***If you have questions about how to meet these guidelines, please contact the program chair before the submission deadline.***

Reviewer Conflict Policy:

During paper submission, all author(s) conflicts must be registered with all possible program committee members. Conflicts are defined as all relationships that would prevent a reviewer from objectively evaluating the submitted work. This includes, but is not limited to, having within the past 5 years: 1) co-authored a publication, 2) shared a funding award, and 3) shared at least one institutional affiliation. ***Note: if a conflict is declared (or left undeclared) in an attempt to manipulate the review process, the submission may be rejected.*** In the situation where the potential conflict is with the program chair, please contact the program chair well before the submission deadline.

Originality of Submissions:

Papers submitted for FPGA 2020 are guaranteed by the authors to be unique manuscripts and not previously published, currently accepted or under consideration for acceptance at another venue. They cannot be substantially similar to any other current/future conference, journal, or workshop submission(s) unless the content appeared at a venue that does not have an archived proceedings.

Rebuttal Process:

FPGA 2020 includes a rebuttal phase for authors to provide an optional response of up to 500-words to reviewers' questions and comments. This information is considered during the final deliberation process. The Rebuttal phase will begin by October 14th and end October 18th.

Author participation:

For inclusion in the ACM digital library, at least one of the authors of each accepted submission is required to attend the conference to present the work.

Best Paper Award and a Special ACM TRETS issue for Best of FPGA 2020

Authors of this year's best manuscripts will be eligible for the conference's best paper awards. They will also be invited to extend their work for consideration in a special issue of ACM's Transactions on Reconfigurable Technology and Systems (TRETS) for FPGA 2020.

NEW: Artifact Evaluation

FPGA 2020 will allow authors to submit accompanying artifacts for their paper submissions for evaluation. This process will allow ACM recognized badges to be associated the final publication. The inclusion of artifacts with a submission is not required for a paper submission nor will any preference be given to submissions with artifacts over those without. Papers and artifacts will be subjected to separate and independent review processes. Artifact evaluation must NOT interfere with the double blind reviewing process of their accompanying papers, so **all accompanying links in the paper to the artifacts should be blinded**. All authors will be required at the time of paper submission to indicate if there will be also be associated artifacts for evaluation. If artifacts will be included, a descriptor of their nature will be required as part of the submission. For more information, go to: http://www.isfpga.org/artifactEvaluation.html.

Important dates:

Abstract Submissions due:	September 9, 2019
Full Paper Submissions due:	September 9, 2019
Final Artifacts for Evaluation due:	September 9, 2019
Author Paper Rebuttals due:	October 18, 2019
Notification of acceptance:	Mid-November, 2019
Camera-ready copy of accepted papers due:	Early December, 2019

Contact Information

For questions about the submission process or technical program:

Lesley Shannon, Program Chair FPGA 2020
ASB 9801, Simon Fraser University
8888 University Dr.
Vancouver BC, V5A 1S6, CANADA
programchair@isfpga.org

For general questions about the conference:

Stephen Neuendorffer, General Chair FPGA 2020
Xilinx
2100 All Programmable Dr.
San Jose, CA 95124, USA
generalchair@isfpga.org

Organizing Committee:

- General Chair: Stephen Neuendorffer, Xilinx, generalchair@isfpga.org .
- Program Chair: Lesley Shannon, Simon Fraser University, programchair@isfpga.org .
- Finance Chair: Kia Bazargan, University of Minnesota, financechair@isfpga.org.
- Artifact Evaluation Co-Chairs: Miriam Leeser, Northeastern University, and Suhaib Fahmy, University of Warwick, artifactevaluationchair@isfpga.org.
- Publicity Chair: Jing Li, University of Wisconsin-Madison, publicitychair@isfpga.org.