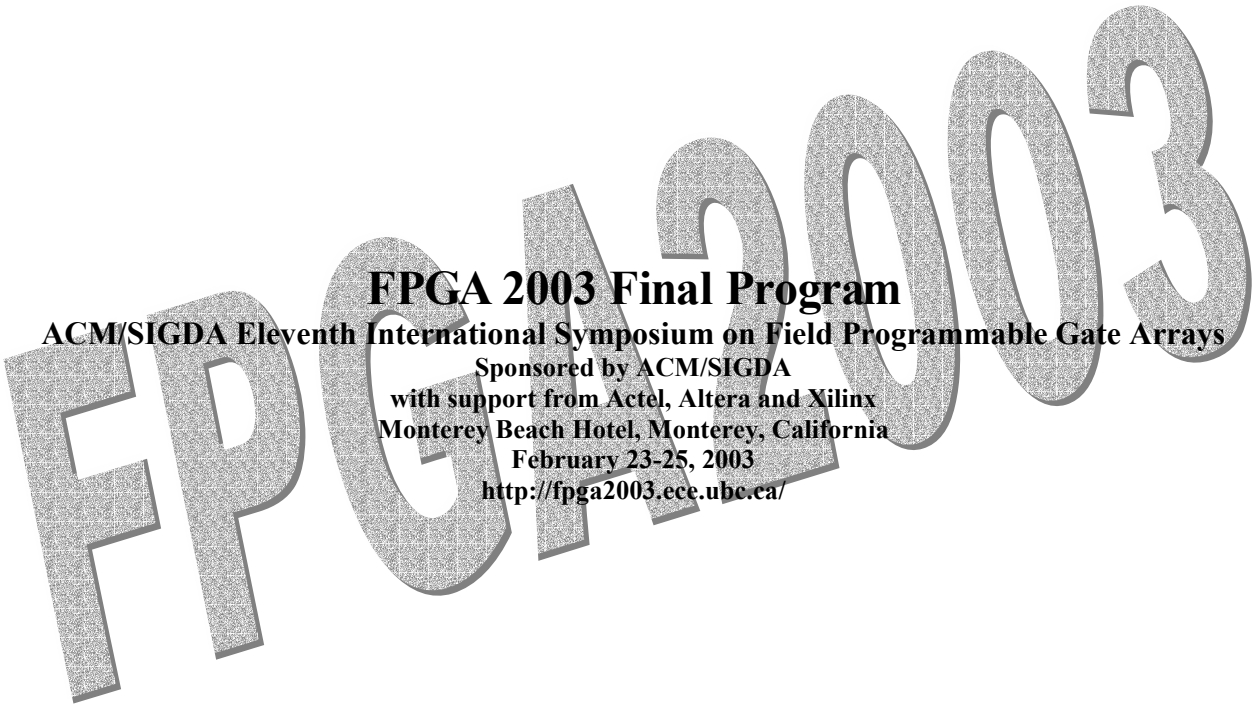


# FPGA 2003 Final Program

**ACM/SIGDA Eleventh International Symposium on Field Programmable Gate Arrays**

**Sponsored by ACM/SIGDA**

**with support from Actel, Altera and Xilinx**

**Monterey Beach Hotel, Monterey, California**

**February 23-25, 2003**

**http://fpga2003.ece.ubc.ca/**

# FPGA 2003 Final Program

## ACM/SIGDA Eleventh International Symposium on Field Programmable Gate Arrays

**Sponsored by ACM/SIGDA**
**with support from Actel, Altera and Xilinx**
**Monterey Beach Hotel, Monterey, California**
**February 23-25, 2003**
**http://fpga2003.ece.ubc.ca/**

Join us at the beach in Monterey, California for the eleventh ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA2003), the premier forum for novel work in all areas related to FPGA technology. This year's FPGA Symposium features twenty-four papers describing cutting-edge FPGA work. Authors present novel work on FPGA architecture from commercial vendors, research labs and universities. Innovative software research highlights high-speed and high-quality FPGA design. Papers also describe novel devices and software for reconfigurable computing. Finally, FPGA 2003 showcases some very impressive applications of FPGAs.

FPGA2003 provides a relaxed environment for informal information exchange, networking and stimulating discussions with the leaders in FPGA research and development from academia and industry. Paper sessions are separated by ample time to peruse the poster presentations and discuss the latest-breaking FPGA news. This year, FPGA 2003 will be held at the Monterey Beach Hotel, a stunning setting guaranteed to facilitate informal discussion as well as formal presentations.

The FPGA 2003 dinner banquet will be followed by a panel discussion. This is an opportunity not to be missed.

If you are at all interested in FPGA technology and developments, you won't want to miss this event.

## Organizing Committee

| | |
|---|---|
| General Chair | Steve Trimberger, Xilinx |
| Program Chair | Russ Tessier, University of Massachusetts - Amherst |
| Publicity Chair | Steve Wilton, University of British Columbia |
| Finance Chair | Martine Schlag, University of California, Santa Cruz |

## Program Committee

| | | |
|---|---|---|
| Ray Andraka, Andraka Consulting | Sinan Kaptanoglu, Altera | Herman Schmit, CMU |
| Vaughn Betz, Altera | Tom Kean, Algotronix | Russ Tessier, U. Mass. - Amherst |
| Michael Butts, Cadence | Arun Kundu, Actel | Steve Trimberger, Xilinx |
| Jason Cong, UCLA | Miriam Leeser, Northeastern U. | Qiang Wang, Xilinx |
| Andre' DeHon, Caltech | Wayne Luk, Imperial College | Steve Wilton, U. British Columbia |
| Eugene Ding, Mentor Graphics | Margaret Marek-Sadowska, UCSB | Martin Wong, UIUC |
| Scott Hauck, U. of Washington | Majid Sarrafzadeh, UCLA | Zeljko Zilic, McGill U. |
| Rajeev Jayaraman, Xilinx | Martine Schlag, UCSC | |

# PROGRAM

## Sunday, February 23, 2003

| | |
|---|---|
| 6:00PM | Registration |
| 7:00PM | Welcoming Reception |

## Monday, February 24, 2003

| | |
|---|---|
| 7:30 AM | Continental Breakfast and Registration |
| 8:20 AM | **Opening Remarks**, Steve Trimberger, Russ Tessier |

### Session 1. **Novel Architectures**

Chair: Michael Butts, Cadence

| | |
|---|---|
| 8:30 AM | **Architectures and Algorithms for Synthesizable Embedded Programmable Logic Cores**, Noha Kafafi, Kimberly Bozman, and Steven J.E. Wilton, University of British Columbia |
| 8:50 AM | **The Stratix Routing and Logic Architecture**, David Lewis, Vaughn Betz, David Jefferson, Andy Lee, Chris Lane, Paul Leventis, Sandy Marquardt, Cameron McClintock, Bruce Pedersen, Giles Powell, Srinivas Reddy, Chris Wysocki, Richard Cliff, and Jonathan Rose, Altera Corporation |
| 9:10 AM | **A Pipelined Configurable Gate Array for Embedded Processors**, Andrea Lodi, Mario Toma, Fabio Campi, Andrea Cappelli, Roberto Canegallo, and Roberto Guerrieri, University of Bologna and STMicroelectronics |
| 9:30 AM | **Coffee Break and Poster Presentations**<br>Poster Session P1. Software and Systems<br>Chair: Herman Schmit, Carnegie Mellon University<br><br>**An Automated and Power-Aware Framework for Utilization of IP Cores in Hardware Generated from C Descriptions Targeting FPGAs,** A. Jones, P. Banerjee, Northwestern U.<br>**Reconfigurable Randomized K-way Graph Partitioning,** Fatih Kocan, Southern Methodist University<br>**Synthetic Circuit Generation Using Clustering and Iteration,** Paul D. Kundarewich, Jonathan Rose, University of Toronto<br>**Design Framework for the Implementation of the 2-D Orthogonal Discrete Wavelet Transform on FPGA,** A. Benkrid, D. Crookes, K. Benkrid**,** The Queen's University of Belfast<br>**Customized Regular Channel Design in FPGAs**, Elaheh Bozorgzadeh, Majid Sarrafzadeh, UCLA<br>**An Estimation and Exploration Methodology from System-Level Specifications : Application to FPGAs**, Sebastien Bilavarn, Guy Gogniat, Jean Luc Philippe, Swiss Federal Institute of Technology, South Britany University<br>**Recursive Circuit Clustering for Minimum Delay and Area**, Mehrdad Eslami Dehkordi, Stephen D. Brown, University of Toronto<br>**An FPGA Architecture with Built-in Error Correction Capability,** P. K. Lala, B. Kiran Kumar, University of Arkansas<br>**A Physical Retiming Algorithm for Field Programmable Gate Arrays**, Peter Suaris, Dongsheng Wang, Pei-Ning Guo, Nan-Chi Chou, Mentor Graphics |

### Session 2. **Placement**

Chair: Vaughn Betz, Altera Corporation

| | |
|---|---|
| 10:30 AM | **Hardware-Assisted Simulated Annealing with Application for Fast FPGA Placement**, Michael G. Wrighton and André DeHon, California Institute of Technology |
| 10:50 AM | **Parallel Placement for Field-Programmable Gate Arrays**, Pak K. Chan and Martine D.F. Schlag, University of California, Santa Cruz |
| 11:10 AM | **I/O Placement for FPGAs with Multiple I/O Standards**, Wai-Kei Mak, University of South Florida |
| 11:30 AM | **Poster Presentations** |

| | |
|---|---|
| 12:00 N | Lunch |

## Session 3. **Routing**

Chair: Jason Cong, UCLA

| | |
|---|---|
| 1:30 PM | **Wire Type Assignment for FPGA Routing**, Seokjin Lee, Hua Xiang, D. F. Wong, Richard Y. Sun, University of Texas at Austin, UIUC, and Xilinx Corporation |
| 1:50 PM | **PipeRoute: A Pipelining-Aware Router for FPGAs,** Akshay Sharma, Carl Ebeling, and Scott Hauck, University of Washington |
| 2:10 PM | **Stochastic, Spatial Routing for Hypergraphs, Trees, and Meshes**, Randy Huang, John Wawrzynek, and André DeHon, University of California, Berkeley and California Institute of Technology |
| 2:30 PM | **Poster Presentations**<br>Poster Session P2. **Applications**<br>Chair: Martine Schlag, UC Santa Cruz<br><br>**FPGA-based Design of an Evolutionary Controller for Collision-free Robot Navigation**, M. A. H. B. Azhar, K. R. Dimond, University of Kent<br>**FPGA Implementation of a Fast Hadamard Transformer for WCDMA**, Sanat Kamal Bahl, Jim Plusquellic, University of Maryland, Baltimore County<br>**A Single-FPGA Implementation of Image Connected Component Labelling**, K. Benkrid, S. Sukhsawas, D. Crookes, S. Belkacemi, The Queen's University of Belfast<br>**Design of a Fingerprint System Using a Hardware/Software Environment**, Lee Vanderlei Bonato, Rolf Fredi Molz, João Carlos Furtado1, Marcos Flores Ferrão, Fernando G. Moraes, UNISC, PUCRS<br>**Implementation of Digital Fixed-Point Approximations to Continuous-Time IIR Filters**, J. E. Carletta, R. J. Veillette, F. W. Krach, Z. Fang, The University of Akron<br>**FPGAs in Critical Hardware / Software Systems**, Adrian J. Hilton, Gemma Townson, Jon G. Hall, Praxis Critical Systems, The Open University<br>**Lattice Adaptive Filter Implementation for FPGA**, Zdenek Pohl, Rudolf Matoušek1, Jirí Kadlec1, Milan Tichý1, Miroslav Lícko. Institute of Information Theory and Automation, CAS<br>**Application-Dependent Testing of FPGAs for Bridging Faults**, Mehdi Baradaran Tahoori, Stanford University<br>**Design Strategies and Modified Descriptions to Optimize Cipher FPGA Implementations: Fast and Compact Results for DES and Triple-DES**, Gaël Rouvroy, Francois-Xavier Standaert, Jean-Jacques Quisquater, Jean-Didier Legat, Université catholique de Louvain |

## Session 4. **Prototyping, Verification, and Test**

Chair: Majid Sarrafzadeh, UCLA

| | |
|---|---|
| 3:30 PM | **Implementation of BEE: A Real-Time Large-scale Hardware Emulation Engine**, Chen Chang, Kimmo Kuusilinna, Brian Richards, and Robert W. Brodersen, University of California, Berkeley and Tampere University of Technology |
| 3:50 PM | **High-Level Modeling and FPGA Prototyping of Microprocessors**, Joydeep Ray and James C. Hoe, Carnegie Mellon University |
| 4:10 PM | **Reducing Pin and Area Overhead in Fault-Tolerant FPGA-based Designs**, Fernanda Gusmão de Lima, Luigi Carro, and Ricardo Reis, Universidade Federal do Rio Grande do Sul |
| 4:30 PM | **Poster Presentations** |

| | |
|---|---|
| 6:00 PM | **Dinner** |
| 7:00 PM - 10:00 PM | **Panel - Attack of the Killer Gate Arrays**<br><br>**Moderator: Michael Butts, *Cadence***<br>**Panelists: Herman Schmit, *Carnegie Mellon University***<br>**Steve Trimberger, *Xilinx***<br>**Jonathan Rose, *Altera***<br>**Ronnie Vasishta, *LSI Logic***<br>**(others panelists TBD)**<br><br>The ever-growing capacity and speed of FPGAs have brought them into the heart of the silicon mainstream. Major ASIC vendors have responded by reviving masterslice gate arrays, standard prefab die with design-specific metal layers. They claim lower NREs, quicker delivery and easier design than cell-based ASICs, and lower unit cost, better speed, capacity and power than FPGAs. Do these gate arrays spell doom for FPGA vendors' dreams of displacing the ASIC as a mainstream silicon platform? Will the FPGA's high volume, superior flexibility and time-to-market prevail? Or will they co-exist in different classes of application? Why? When?<br><br>We have assembled a panel of experts from FPGA and ASIC vendors and academia to duke it out. Each panelist will give a short presentation putting forward their point of view, then we'll have interactive debate among the panelists and attendees. |

# Tuesday, February 25, 2003

| | |
|---|---|
| 7:30 AM | Breakfast |

## Session 5. **Logic Synthesis and Mapping**

Chair: Steve Wilton, University of British Columbia

| | |
|---|---|
| 8:30 AM | **Placement-driven Technology Mapping for LUT-based FPGAs**, Jason Cong, Ashok Jaganathan, and Joey Y. Lin, UCLA |
| 8:50 AM | **Verifying the Correctness of FPGA Logic Synthesis Algorithms**, Boris Ratchev, Mike Hutton, Gregg Baeckler, and Babette van Antwerpen, Altera Corporation |
| 9:10 AM | **Using Logic Duplication to Improve Performance in FPGAs**, Karl Schabas and Stephen D. Brown, University of Toronto |
| 9:30 AM | **Coffee Break and Poster Presentations**<br>Poster Session P3. **Architecture**<br>Chair: Andre' DeHon, Caltech<br><br>**A High-speed Successive Erasure BCH Decoder Architecture**, Thomas Buerner, Friedrich-Alexander University of Erlangen-Nuremberg<br>**Track Placement: Orchestrating Routing Structures to Maximize Routability**, Katherine Compton, Scott Hauck, Northwestern University, University of Washington<br>**A SC-based Novel Configurable Analog Cell**, Binlin Guo, Jiarong Tong, Fudan University<br>**Reconfigurable CDMA Receiver Architecture for 3G Mobile Terminals**, Mario Nicola, Andrea Molino, Guido Masera, Politecnico di Torino<br>**A High Resolution Diagnosis Technique for Open and Short Defects in FPGA Interconnects**, Mehdi Baradaran Tahoori, Stanford University<br>**A Four-bit Full Adder Implemented on Fast SiGe FPGAs with Novel Power Control Scheme**, K. Zhou, M. Chu, C. You, J.-R. Guo, Channakeshav, J. Mayega, B.S. Goda, R.P. Kraft, J.F. McDonald, Rensselaer Polytechnic Institute<br>**Testing for Bit Error Rate in FPGA Communication Interfaces**, Yongquan Fan, Zeljko Zilic, McGill University |

## Session 6. **Device-Level Design**

Chair: Guy Lemieux, University of British Columbia

| | |
|---|---|
| 10:30 AM | **A Scalable 2V, 20 GHz FPGA using SiGe HBT BiCMOS Technology**, J.R. Guo, C. You, K. Zhou, M. Chu, B.S. Goda, R.P. Kraft, and J.F. McDonald, Rensselaer Polytechnic Institute |
| 10:50 AM | **Design of FPGA Interconnect for Multilevel Metalization**, Raphael Rubin and André DeHon, California Institute of Technology |
| 11:10 AM | **Automatic Transistor and Physical Design of FPGA Tiles from an Architectural Specification**, Ketan Padalia, Ryan Fung, Mark Bourgeault, Aaron Egier, and Jonathan Rose, University of Toronto |
| | **Poster Presentations** |

| | |
|---|---|
| 12:00 N | Lunch |

## Session 7. **Architecture Analysis and Evaluation**

Chair: Sinan Kaptanoglu, Altera Corporation

| | |
|---|---|
| 1:30 PM | **Architecture Evaluation for Power-Efficient FPGAs,** Fei Li, Deming Chen, Lei He, and Jason Cong, UCLA |
| 1:50 PM | **Post-Placement C-slow Retiming for the Xilinx Virtex FPGA**, Nicholas Weaver, Yury Markovskiy, Yatish Patel, and John Wawrzynek, University of California, Berkeley |
| 2:10 PM | **An FPGA Architecture with Enhanced Datapath Functionality**, Katarzyna Leijten-Nowak and Jef L. van Meerbergen, Eindhoven University of Technology and Philips Research Labs |
| 2:30 PM | **Coffee Break and Poster Presentations**<br>Poster Session P4. **Reconfigurable Computing**<br>Chair: Katherine Compton, Northwestern University<br><br>**Making Area-Performance Tradeoffs at the High Level Using the AccelFPGA Compiler for FPGAs**, P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, R. Anderson, AccelChip<br>**A Logic Based Approach to Hardware Abstraction,** K. Benkrid, S. Belkacemi, D. Crookes, The Queen's University of Belfast<br>**A Granularity-based Classification Model for Systems-on-a-Chip**, Stephan Bingemer, Peter Zipf, Manfred Glesner, Darmstadt University of Technology<br>**Using FPGAs for Data and Reorganization Engines: Preliminary Results for Spatial Pointer-based Data Structures,** Pedro C. Diniz, Joonseok Park, USC/ISI<br>**On Hiding Latency in Reconfigurable Systems: The Case of Merge-Sort for an FPGA-Based System,** Hossam ElGindy, George Ferizis, The University of New South Wales<br>**On Computation and Resource Management in an FPGA-based Computation Environment,** Soheil Ghiasi, Karlene Nguyen, Elaheh Bozorgzadeh, Majid Sarrafzadeh, UCLA<br>**Wireless Sensor Networks: a Power-Scalable Motion Estimation IP for Hybrid Video Coding**, Federico Quaglio, Maurzio Martina, Fabrizio Vacca, Guido Masera, Andrea Molino, Gianluca Piccinini, Maurizio Zamboni, Politecnico di Torino |

## Session 8. **Innovative Applications**

Chair: Ray Andraka, Andraka Consulting Group

| | |
|---|---|
| 3:30 PM | **A Fully Pipelined Memoryless 17.8 Gbps AES-128 Encryptor**, Kimmo U. Järvinen, Matti T. Tommiska and Jorma O. Skyttä, Helsinki University of Technology |
| 3:50 PM | **Methodology to Implement Block Ciphers in Reconfigurable Hardware and its Application to Fast and Compact AES RIJNDAEL**, Francois-Xavier Standaert, Gael Rouvroy, Jean-Jacques Quisquater, and Jean-Didier Legat, Université catholique de Louvain |
| 4:10 PM | **Energy-Efficient Signal Processing Using FPGAs**, Seonil Choi, Ronald Scrofano, Viktor K. Prasanna, and Ju-wook Jang, University of Southern California |

| | |
|---|---|
| 4:30 PM | **Closing Remarks,** Steve Trimberger, Russ Tessier |

# Hotel Reservations

FPGA 2003 will be held at the Monterey Beach Resort. Attendees who will be staying at the hotel must make hotel reservations in addition to their conference registration. To make reservations at the hotel, contact:

**The Beach Resort**
**2600 Sand Dunes Drive**
**Monterey, CA 93940**
**USA+831-394-3321**
**http://www.montereybeachresort.com**

Tell them that you are with the **ACM/FPGA** conference to get the conference rate of $112 Gardenside or $162 Oceanside. The room rate is the same for single or double. The conference cut off-date is February 8, 2003. Reservations received after February 8 will be accepted on a space and rate available basis only.

For information on the Monterey area, visit the Web site: http://www.gomonterey.com/

# REGISTRATION FORM FOR FPGA'03

## ACM/SIGDA International Symposium on Field Programmable Gate Arrays

**February 23-25, 2003 Monterey, California, USA**

**To register on the web, go to** https://campus.acm.org/register/fpga03/

Name (first, middle, last): _____

Affiliation (for badge): _____

Title/Job Function: _____

Address: _____

City: _____ State: _____ Zip Code: _____

Country: _____ Email: _____

Phone: (____)_____ Fax: (_____)_____

ACM/SIG Member ID: _____ Student ID: _____

Special Needs:_____ Special Dietary Requirements: Vegetarian Kosher Vegan

Do not include my name, address and e-mail id in the conference attendee listing _____.

***PLEASE NOTE: Conference*** *registration fee includes one copy of the conference proceedings, 2 continental breakfasts, 2 lunches, one ticket to Sunday's Reception and one ticket to Monday's Dinner.*

**REGISTRATION FEES** (Please circle appropriate fees)

*The cut off date for preregistration is February 14, 2003. After this date you must register on-site.*

| | **Registration on or Before 1/24/03** | | | **Registration after 1/24/03** | | |
|---|---|---|---|---|---|---|
| | *Member* | *Non-Member* | *Student* | *Member* | *Non-Member* | *Student* |
| FPGA'03 Conference | $325.00 | $425.00 | $ 85.00 | $400.00 | $500.00 | $ 95.00 |

**Extras:**

Guest *Monday Dinner* Tickets: ____ tickets x $60 = _____

Total Fees: US $_____ (**Make checks payable to ACM/FPGA'03 Conference**)

Payment included (circle one): American Express Master Card Visa Check

Credit Card Number: _____ Expiration Date: _____

Names as it appears on Credit Card: _____

Signature: _____

For questions (8:30 am - 4:30 PM EST), Email: acmhelp@acm.org Telephone: (US and Canada) 1-800-342-6626, (outside the US) 1-212-626-0500. For Credit Card payments, Fax 1-212-944-1318,. **If paying by check, mail check with registration forn to:**

ACM Member Services, P.O. Box 11405, New York, NY 10286-1405, USA

Cancellations must be received in writing by contacting the ACM Member Services Department. A US $50 cancellation fee will be charged. **You should receive e-mail confirmation within 3 business days. If you do not please contact our member services department at the above contact information.**

*Remember, if you are planning to stay at the conference hotel, you must ALSO make a hotel room reservation: USA+831-394-3321* http://www.montereybeachresort.com/