Spatial Debug & Debug without re-programming in Microsemi FPGAs

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Agenda

- ❑Traditional debug methods and challenges
- ❑Our Solutions
  - ❑Debug without re-programming
  - ❑Spatial Debug
- ❑Illustrative Examples
- ❑Conclusions

Debug Challenges

- SoCs are complex
  - soft IP
  - hard IP
  - firmware IP

"conservatively, 35% to 50% of time is spent in debug and it could go beyond that depending on the state or size of the project." [*Semiconductor Engineering, 2016*]

Source: http://semiengineering.com/debug-last-bastion-of-automation/

Top FPGA Prototyping Challenges [*Synopsys Survey 2013*]

1. **Mapping ASIC Into FPGAs**
2. **Clocking Issues**
3. **Debug Observability**

Source: https://blogs.synopsys.com/breakingthethreelaws/2013/03/fpmm-downloads-surpass-3500-copies-do-you-have-a-copy/

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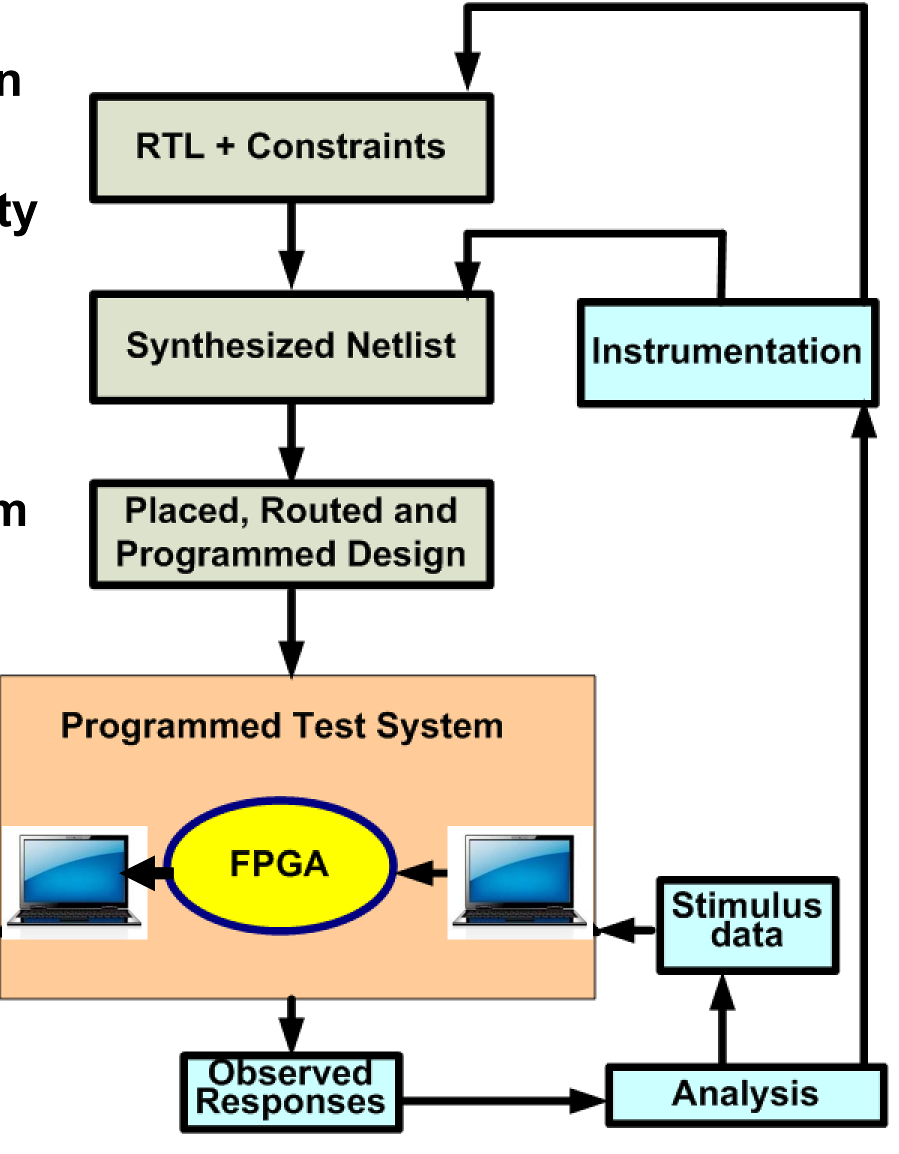
What makes Debug so painful ?

- Too many debug cycles
  - Limited observability in each iteration
  - Limited or no controllability
  - Instrumentation affects reproducibility
- Each cycle is too long
  - Need to re-run place and route
  - Must re-establish timing closure
  - Requires re-programming and system restart



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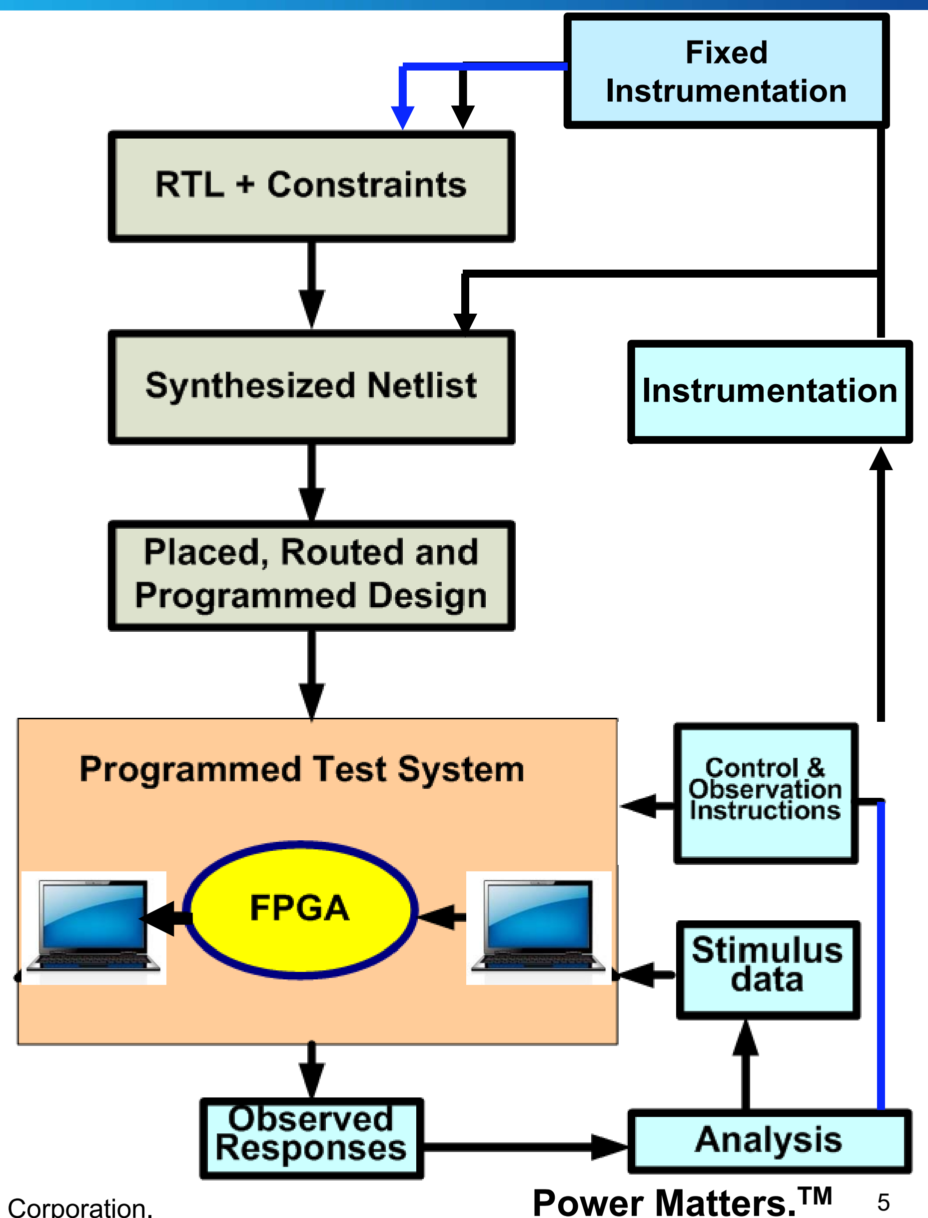
Microsemi Debug Solution

- Observability
  - Dynamically addressable probe
  - Snapshot
  - Peek memory
- Controllability
  - Write probe
  - Poke memory
- Shorter cycles
  - No need for new RTL
  - Reproducibility



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Terminology on Instrument Elements

Static: can be created and destroyed only at the FPGA design time, i.e. requires FPGA design time instrumentation + re-programming

Dynamic: can be created and destroyed on the fly during the normal operation of the DUT, i.e. no design-time re-instrumentation, no FPGA re-programming needed

In-situ: measurement can be taken in the same place the phenomenon is occurring without isolating it from other systems or altering the original conditions of the test, i.e. DUT and stimulus vector continue un-interrupted

External: can be observed/controlled with an external agent such as an oscilloscope or JTAG or SPI master

Internal: can be observed/controlled with an internal agent such as an integrated (on-chip) logic analyzer, or embedded processor

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Live Probe with Feedback

DUT

D SET Q CLR Q

RAM

Internal Soft Instrumentation

JTAG

LIVE PROBE A

LIVE PROBE B

SmartDebug

LIVE PROBE
- **for observability:**
  - **2 probes available**
  - **dynamic, in-situ, external**

LIVE PROBE FEEDBACK
- **for controllability:**
  - **no limit on feedbacks**
  - **static, in-situ, internal**

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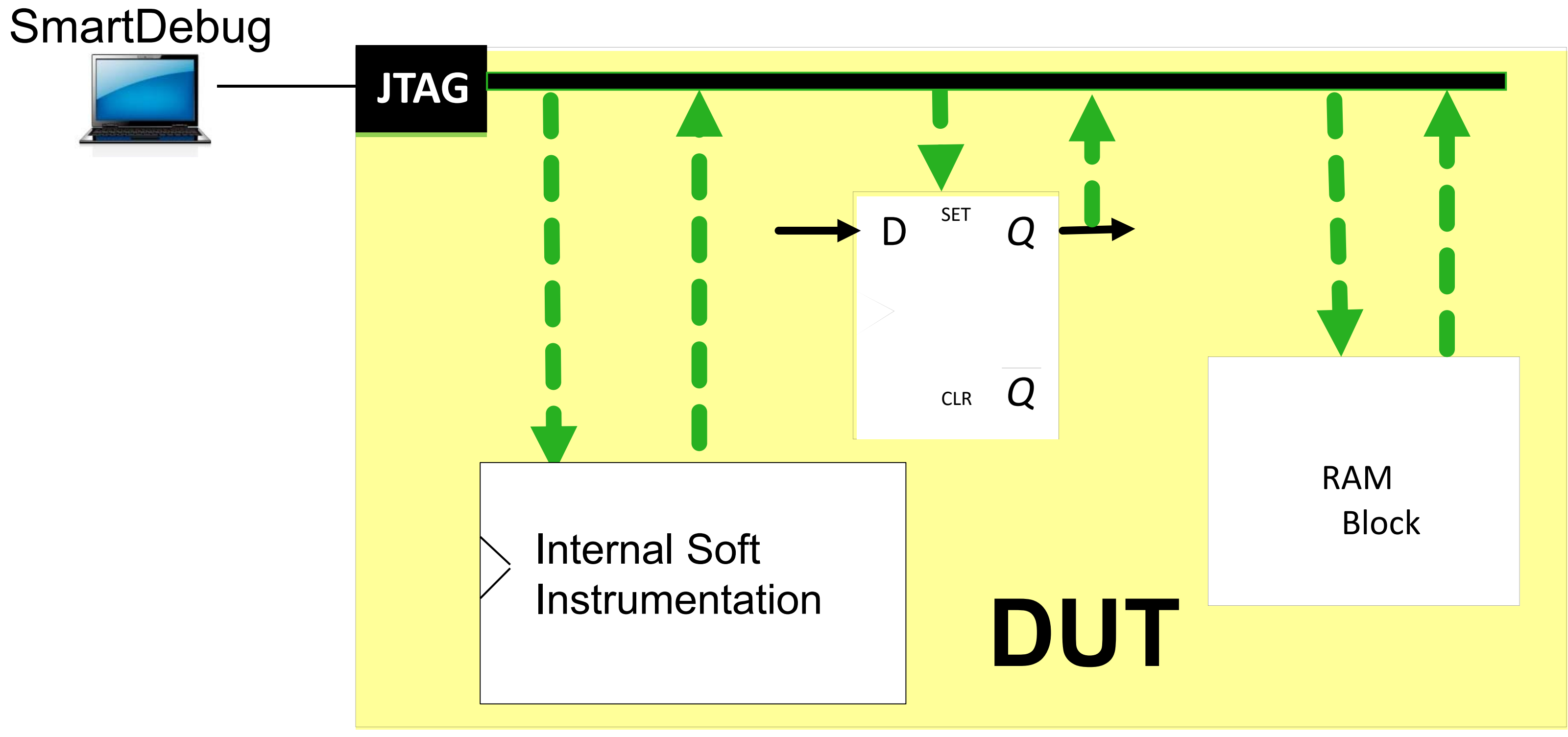
Active Probe and Memory Peek/Poke



Observability
- **Sample Register**
- **Peek Memory Address**
- **dynamic, in-situ, external**

Controllability
- **Set Register**
- **Poke Memory Address**
- **dynamic, in-situ, external**

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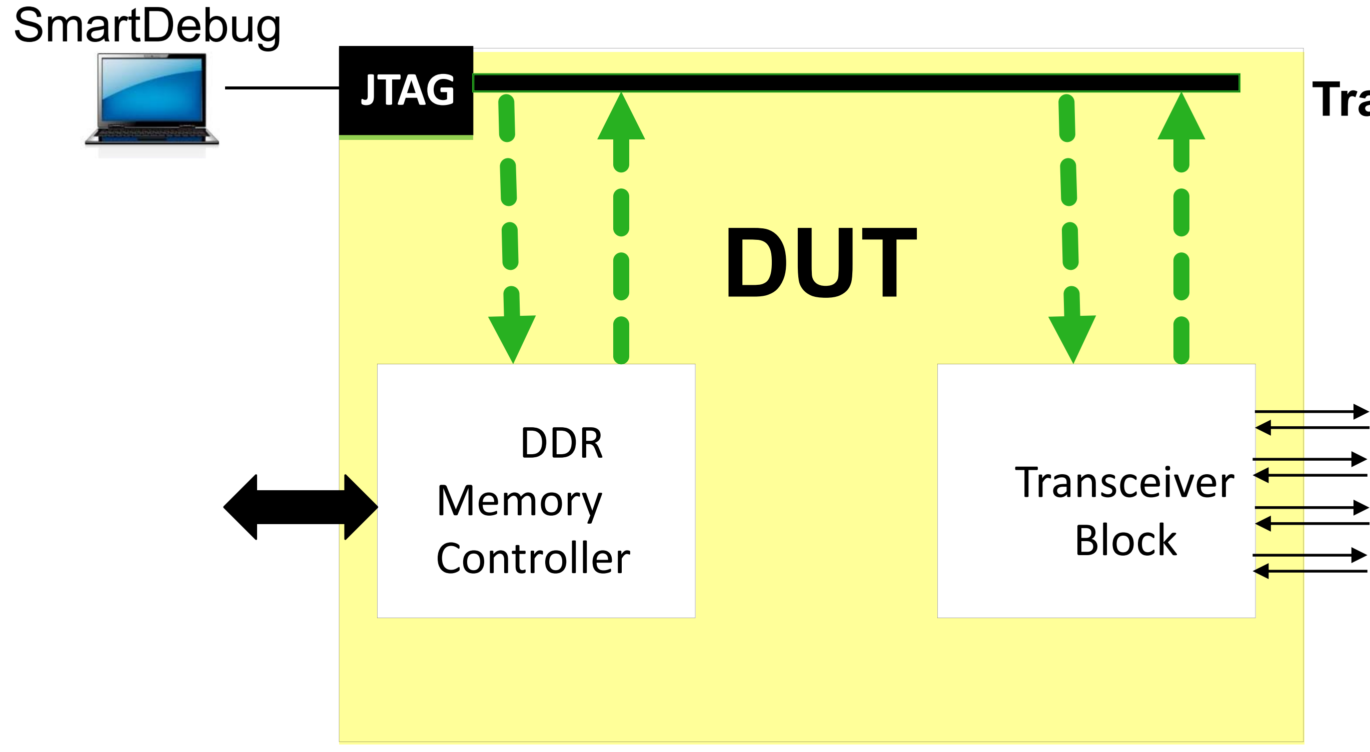
Peripheral Peek/Poke



Transceiver Block

- **Protocol**
- **PMA Ready/ RX & TX PLL status**
- **PRBS traffic generation and BER monitoring**
- **Configuring Loopbacks, PLLs**
- **Register Peek and Poke**
- **SERDES System, PMA Lane and**
- **PCIeCore registers**

DDR Memory Controller

- **Peek & Poke Controller registers**
- **dynamic, in-situ, external**

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Example: Event Counter

DUT

D

A

Q

D

B

Q

'1'

'0'

LIVEPROBE
COUNTER
C1

JTAG

= 0

SmartDebug

Register A is toggling
Register B is stuckat '0'
Register B is forced to '1'

- Reset (de-) / assertion
- Clock not toggling
- Stuck-at-fault register
- Interrupts not getting asserted or asserting too often

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Active Probe Read, Modify, Write

Live/Active Probes Selection

Hierarchical View | Netlist View

Filter: Search

Instance(s): Add

Instance Tree
- COREFIFO_1
- Clocks_In_0
- DFN1C0_0
- DFN1C0_1
- DFN1C0_2
- DFN1C0_3
- DFN1C0_4
- ERROR_packet
- ItchyScratchy_0
- One_Hot_SM_0
- PACKET_MONITOR_0
- SHIFT_PACKET_0
- count2_0
- count_0

FPGA Array debug data

Live Probes | Active Probes | Memory Blocks | Probe Insertion

Select Active Probe tab

Save... Load... Delete Delete All

Name	Type	Read Value	Write Value
count_0_coutB[15:0]	DFF	16'h85CE	16'h
coutA_0_c[7:0]	DFF	8'hE2	8'h90

Read Active Probes | Write Active Probes

Search / Select signal(s) from the design

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Live Probe

Live/Active Probes Selection

Hierarchical View | Netlist View

Filter: Search

Instance(s): Add

Instance Tree
- COREFIFO_1
- Clocks_In_0
- DFN1C0_0
- DFN1C0_1
- DFN1C0_2
- DFN1C0_3
- DFN1C0_4
- ERROR_packet
- ItchyScratchy_0
- One_Hot_SM_0
- PACKET_MONITOR_0
- SHIFT_PACKET_0
- count2_0
- count_0

FPGA Array debug data

Live Probes | Active Probes | Memory Blocks | Probe Insertion

Select Live Probe tab

Delete | Delete All

Name	Type
CLK_OUT_1_c:Clocks_In_0/CLK_DIV_2_1/CLK_OUT:Q	DFF
CLK_OUT_3_c:Clocks_In_0/CLK_DIV_2_3/CLK_OUT:Q	DFF

Assign to Channel A -> CLK_OUT_1_c:Clocks_In_0/CLK_DIV_2_1/CLK_OUT:Q

Assign to Channel B ->

Unassign Channels

Search / Select signal(s) from the design

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Memory Peek, Modify and Poke

Memory Blocks Selection

FPGA Array debug data

Memory Blocks: Select

COREFIFO_1/genblk20.UI_ram_wrapper

Live Probes | Active Probes | Memory Blocks | Probe Insertion

Select Memory Blocks tab

Current Memory Block: COREFIFO_1/genblk20.UI_ram_wrapper_1/U2_asyncnonpipe/top_itchy_sratchy_COREFIFO_1_USRAM_top_R0C0/INST_RAM64x18_IP

Data bit Mode: 9

ADDR															
0000	083	016	1C2	016	1C3	016	1C4	016	1C5	016	1C6	016	1C7	096	1C8
0010	1C9	016	1CA	016	1CB	016	1CC	016	1CD	016	1CE	016	1CF	096	1D0
0020	1D1	016	1D2	016	1D3	016	1D4	016	1D5	016	1D6	016	1D7	096	1D8
0030	1D9	016	1DA	016	1DB	016	1DC	016	1DD	016	02D	016	1DF	096	1E0
0040	1E1	016	1E2	016	1E3	016	1E4	016	1E5	016	0FF	016	1E7	096	1E8
0050	1E9	016	1EA	016	1EB	016	1EC	016	1ED	016	1EE	016	1EF	096	1F0
0060	1F1	016	1F2	016	1F3	016	1F4	016	1F5	016	1F6	016	1F7	096	1F8
0070	1B9	016	1BA	016	1BB	016	1BC	016	1BD	016	1BE	016	1BF	096	1C0

Read Block | Write Block

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Example: Frequency Meter

F1
D Q
Q
F4
D Q
Q
F ref
REFERENCE COUNTER C0
Control Logic
LIVEPROBE COUNTER C1
DUT clocks
JTAG
SmartDebug

Is the clock toggling @ expected frequency ?

$$F_4 = 2\left(\frac{C1}{C0}\right)F_{ref}$$

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Execution Control with FPGA H/W Breakpoint

HALT & RUN request from uP

Trigger

Controlled via chip JTAG

SmartDebug

HALT

RUN

STEP

FPGA H/W Breakpoint

(FHB) Block

(~ 200 LUTs & Registers)

RUN request to uP

Halt request to uP

CLK_EN

Clock Control Circuit (CCC)

Clocks to DUT

FHB uses up soft gates and registers and accounts for ~ 1% overhead

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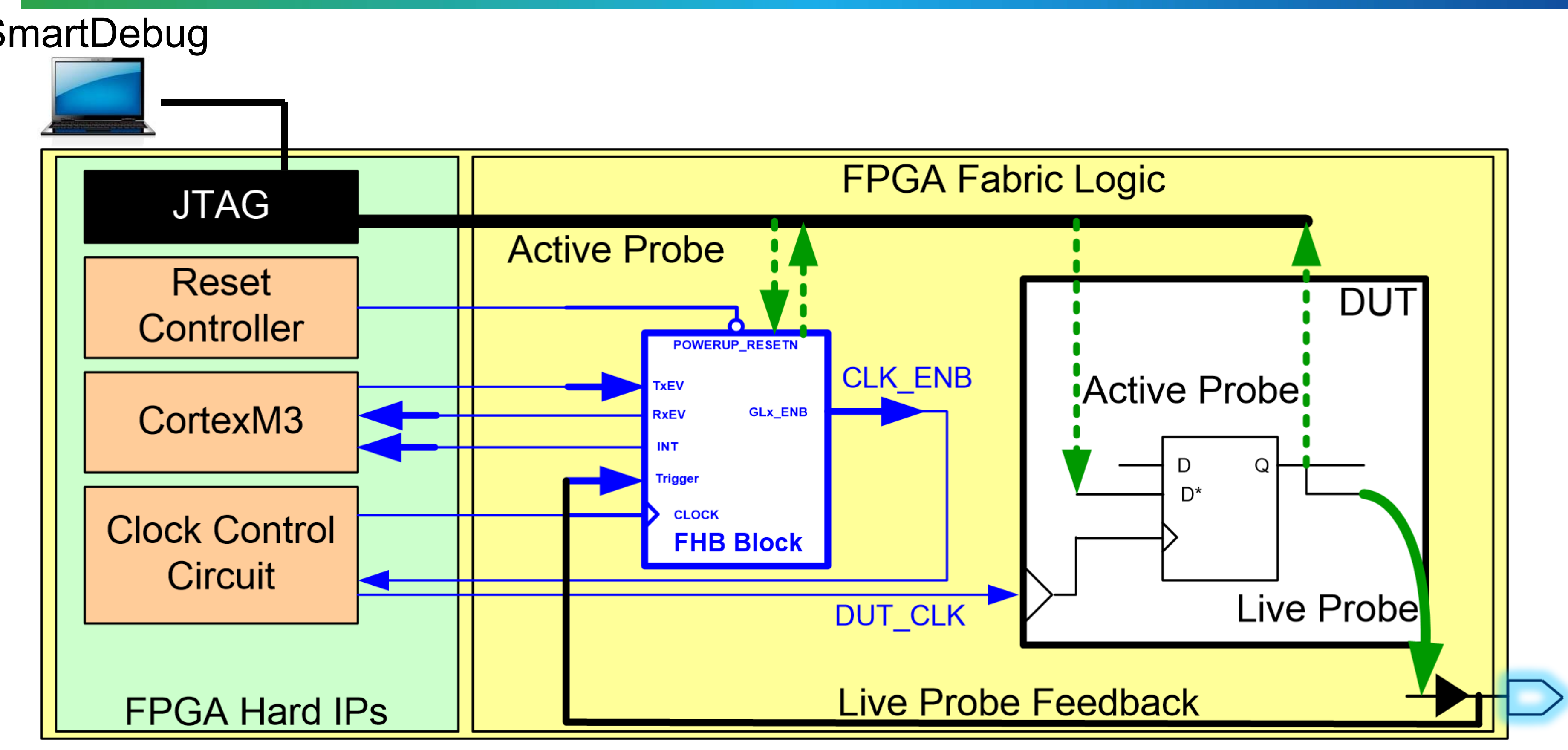
Spatial Capture - Data Acquisition



1. Observe Initial state of DUT: (optional)
   - With DUT held in reset, use forced trigger to halt DUT
   - Read values from registers, latches and memories represents the initial state
2. Observe interesting state of DUT:
   - Use LiveProbe Feedback to trigger HALT DUT + CortexM3 firmware
   - Read values from registers, latches and memories at the falling or rising edge of the trigger

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Example: Ethernet Datapath Dies

FHB → RUN

EMPTY

Packet Write FSM — Write Data → FIFO — Read Data → Packet Read FSM

Write_EN

Read_EN

Ingress packet counter is incrementing

Egress packet counter stops incrementing

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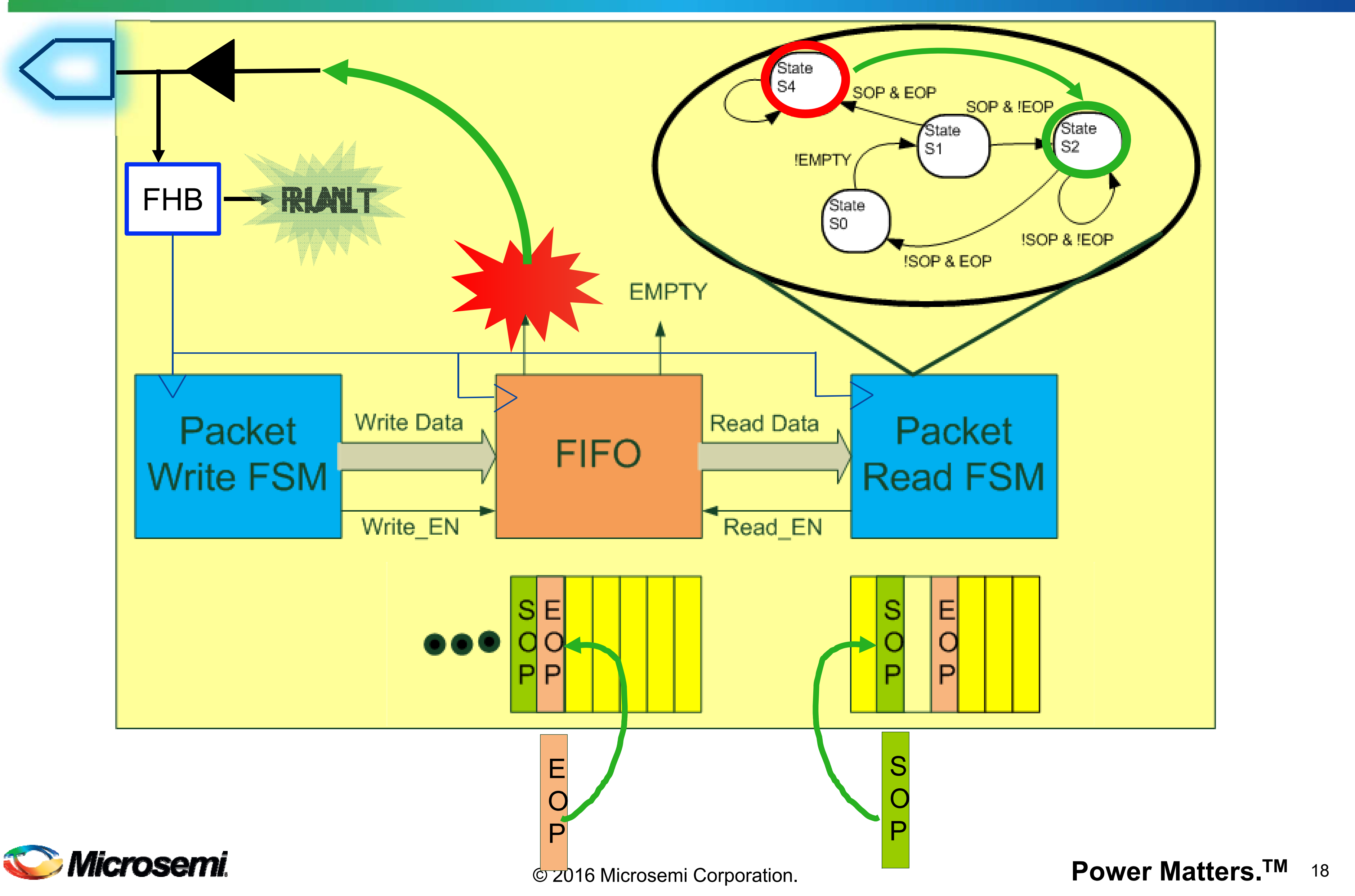
Example: FIFO overflow



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Example: Ethernet Datapath Recovered Root-cause Found

FHB

RUN

FULL

EMPTY

Packet Write FSM

Write Data

Write_EN

FIFO

Read Data

Read_EN

Packet Read FSM

Ingress packet counter is incrementing

Egress packet counter is incrementing

Summary

Features	Microsemi SmartDebug
Dynamic, in-situ signal probing	●
Dynamic, in-situ trigger selection	●
Dynamic, in-situ Event counter, Frequency Meter	●
Register Observability	●
Memory Observability	●
Register Controllability	●
Memory Controllability	●

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