Boolean Satisfiability-Based Routing and Its Application to Xilinx UltraScale Clock Network

Henri Fraisse Abhishek Joshi

Dinesh Gaitonde Alireza Kaviani

Xilinx Inc.

{Henri.Fraisse, Abhishek.Joshi, Dinesh.Gaitonde, Alireza.Kaviani}
@xilinx.com

Agenda

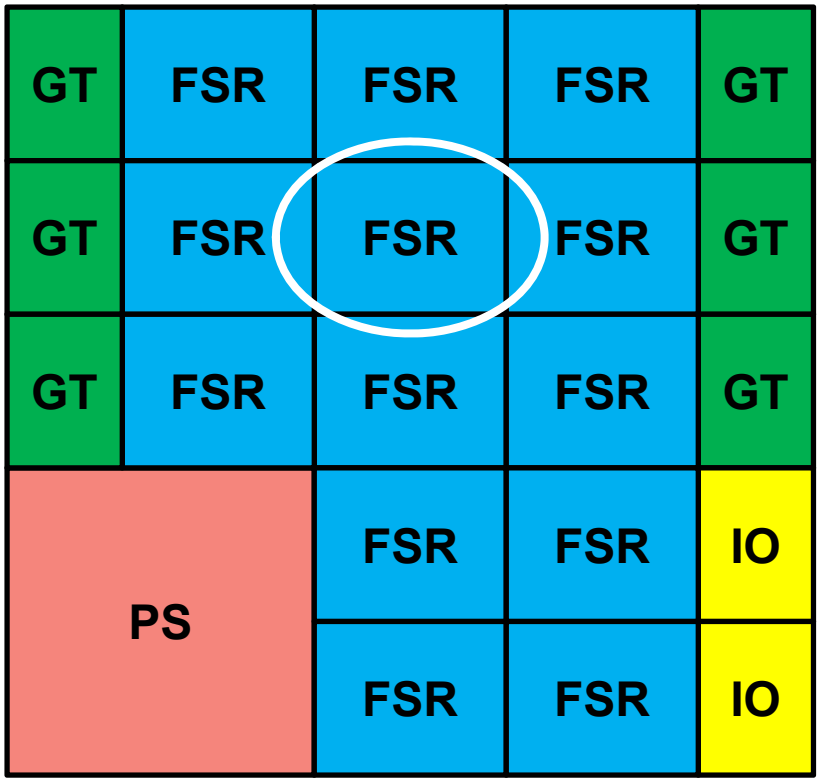
- Introduction
- UltraScale clocking architecture
- Vivado clock routing
- Comparison of routing algorithms
- Conclusion

Clock routing challenges in modern FPGA

- The clocking resources of modern FPGAs are rapidly increasing in both size and complexity
  - More than 600 clocking buffers in the largest Xilinx UltraScale devices
- Conventional routing algorithms are running out of steam
  - Routability issues are emerging during clock tree synthesis
- New routing algorithms are required
  - SAT-based routing is proposed to address these challenges

UltraScale clocking architecture

A simplified Zync UltraScale device

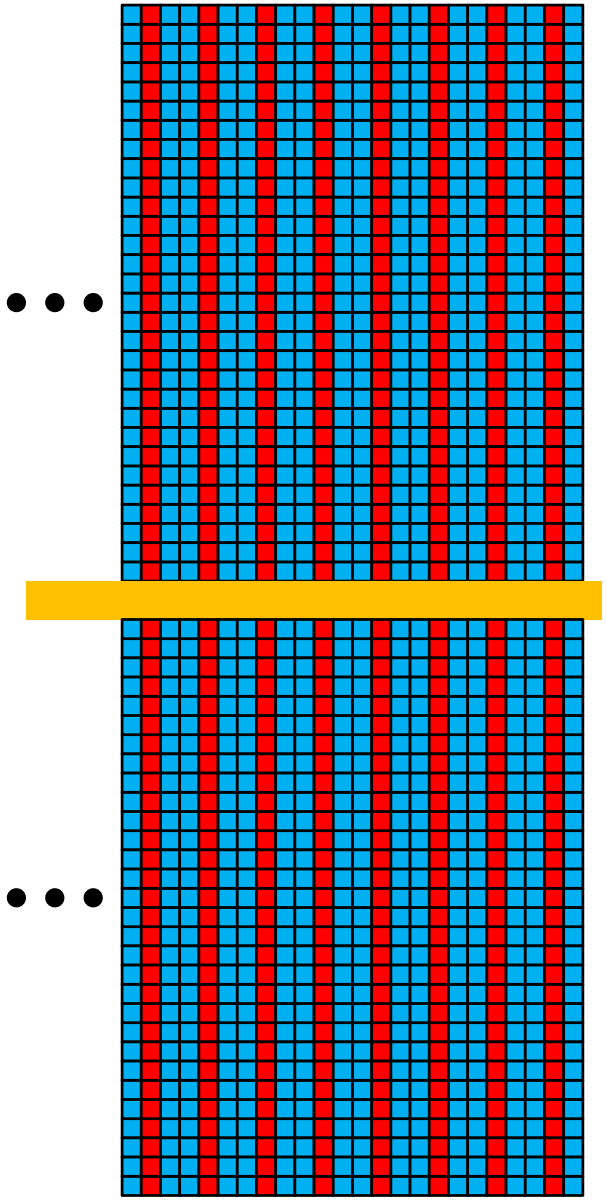


FSR: Fabric Sub Region

GT: Gigabit Transceiver

PS: Processor Sub System

Under the hood of a Fabric Sub Region

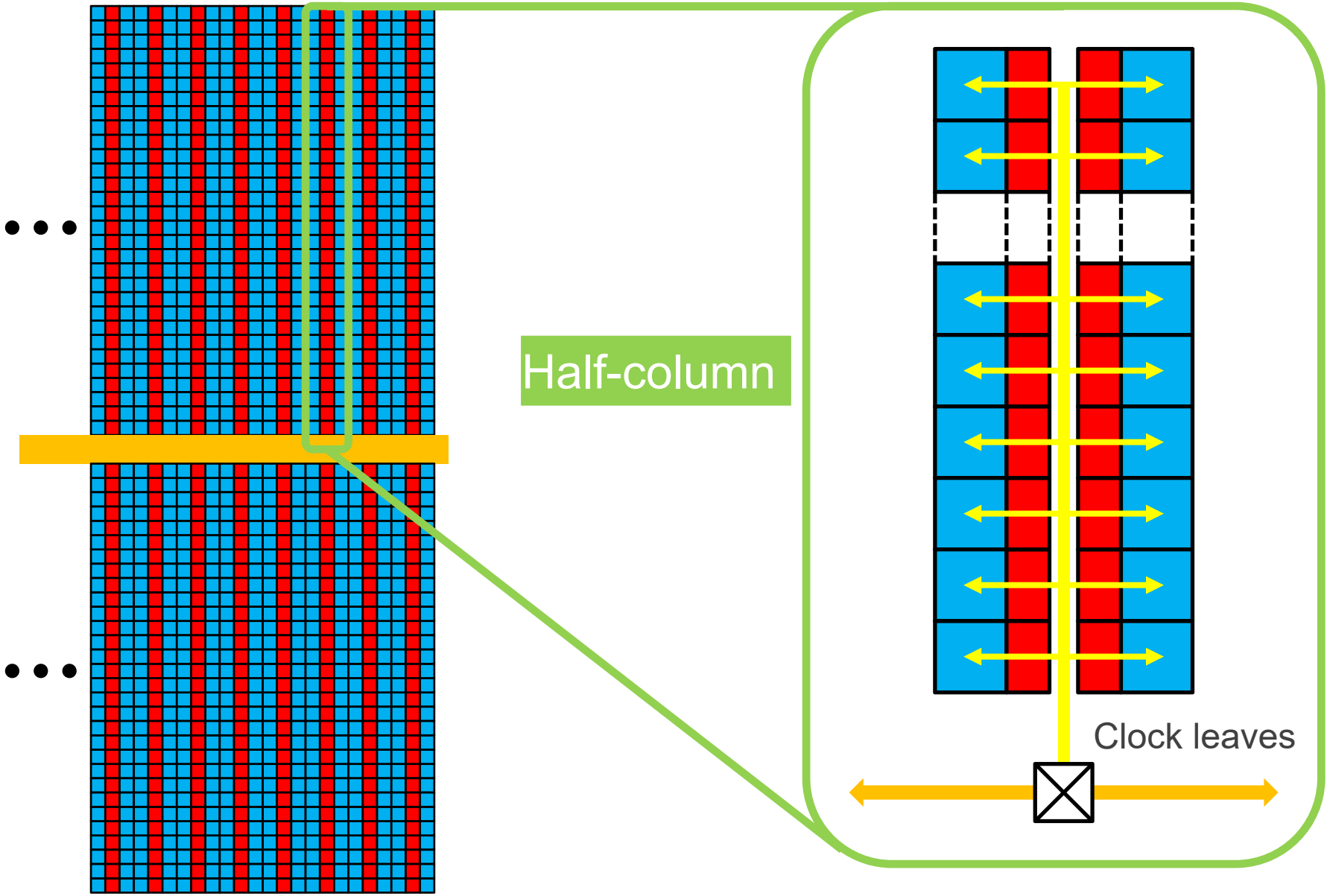


Half FSR

Clocking resources

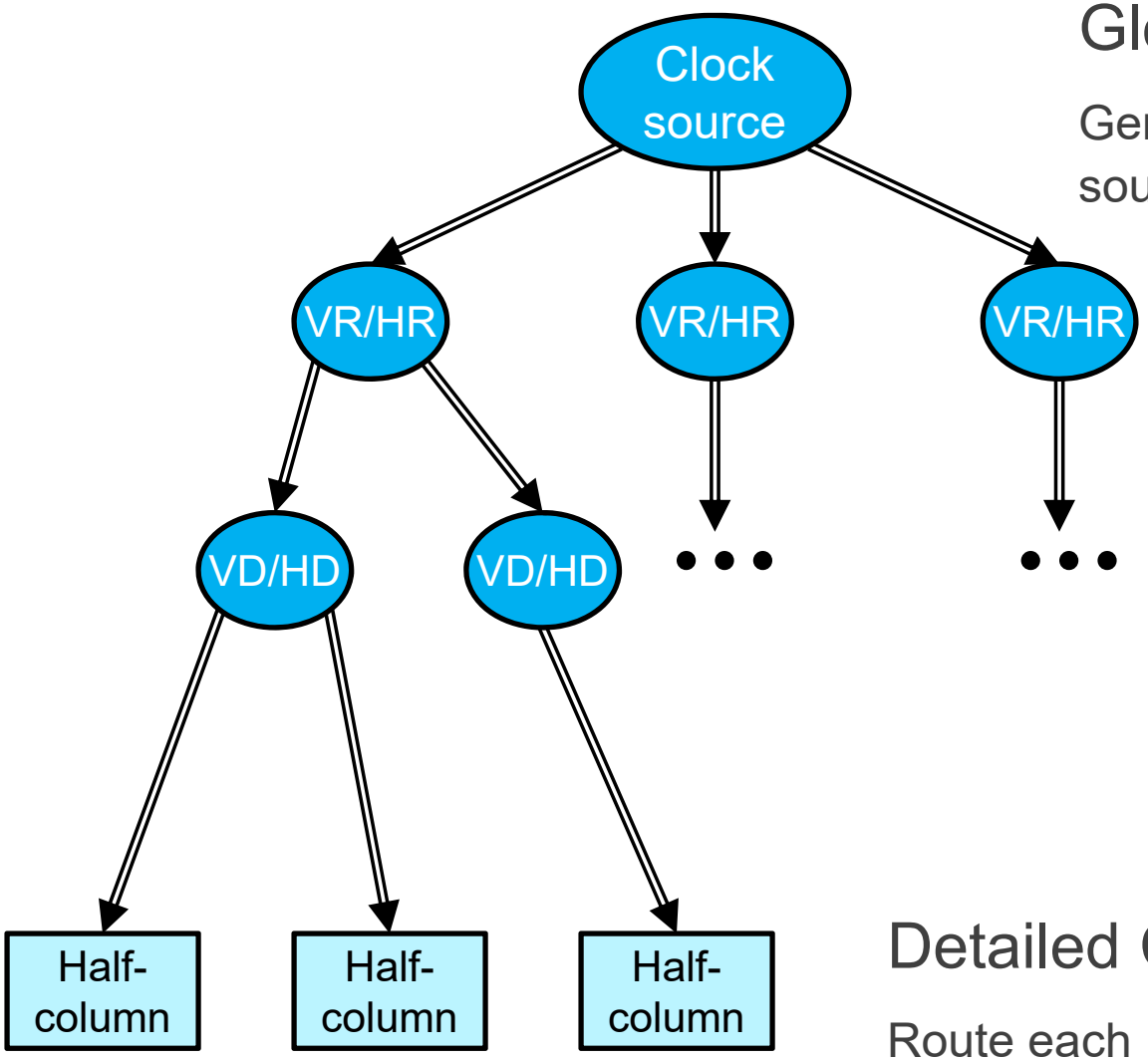
- Interconnect Tile
- Configurable Logic Block (LUT, FF)

Under the hood of a Fabric Sub Region



Vivado clock routing

Clock routing



Global Clock Routing:

Generate partial tree from clock sources to Half-columns

Detailed Clock Routing:

Route each Half-column

Comparison of routing algorithms

SAT routing versus Iterative algorithms

- Created more than 1000 designs to stress clock routing
- Extracted the 51 designs not fully routed with standard iterative routing algorithms
- Collected the 1803 unsolved routing problems

	Designs	Routing problems
Total	51	1803
Routed SAT	43 (84.3%)	1786 (99.0%)

SAT-based routing can route efficiently 99% of the clock routing problems unsolved with iterative algorithms

Comparison of two SAT encodings

	Binary	Unary
Initial number of variables	LOW	HIGH
Additional variables for CNF	MANY	NO
Reduction of variables from graph reachability	NO	YES

	Binary	Unary	Avg. of ratios
Avg. runtime	1.4 sec	0.13 sec	17.9
Avg. variable count	10226	990	10.2
Avg. clause count	51494	3102	16.5
Avg. literal count	150780	7500	19.9

Unary SAT encoding is 18 times faster and produces formulas 20 times smaller

Concluding Remarks

- Improved Vivado clock routing using SAT-based routing
  - Both Routability and Runtime
- Demonstrated that Unary encoding is more efficient than conventional Binary encoding
  - Evaluated two SAT encodings and provided a comparative analysis
- Exploring SAT-Based routing for other applications

Thank you!