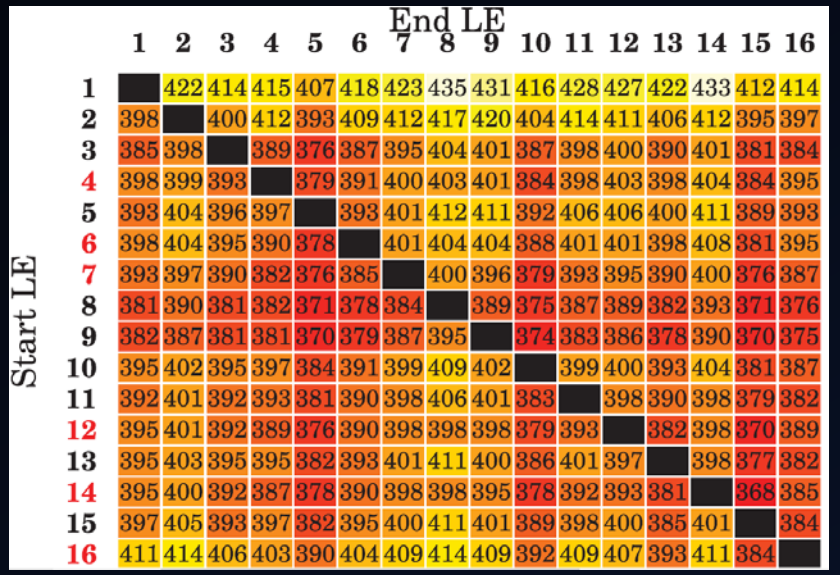
Pitfalls & Trade-offs in Simultaneous, On-Chip FPGA Delay Measurement

Timothy Linscott, Raphael Rubin,
Benjamin Gojman, André DeHon

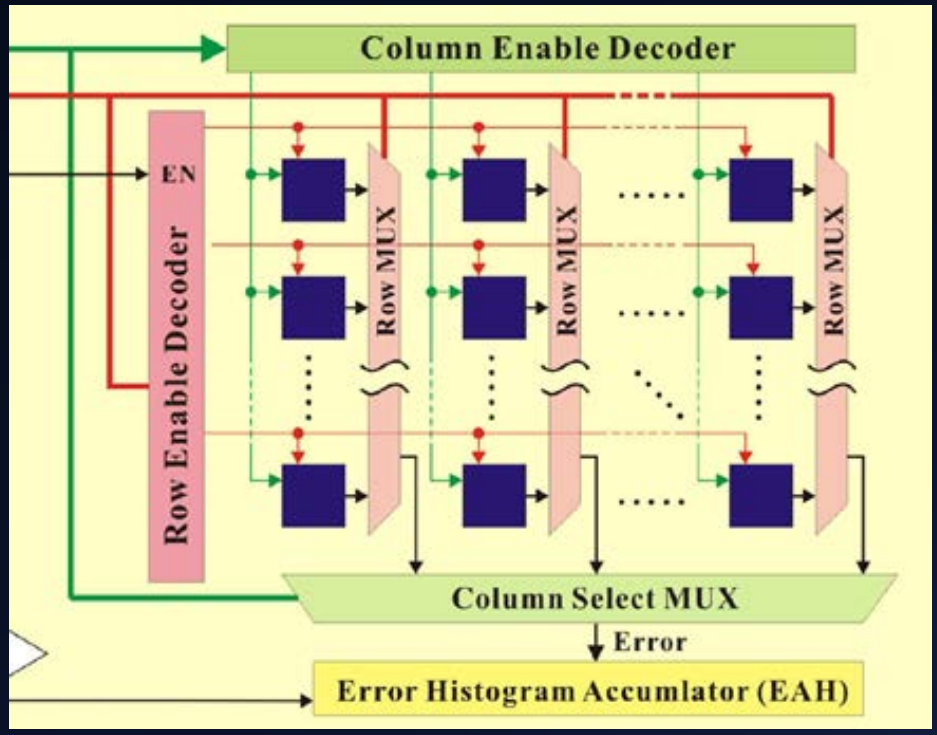
FPGA 2016

FPGA Self-Measurement

- Map component delays
- Previous FPGA measurement work
  - Imperial, 2009
  - Penn, 2014
- Is parallel measurement accurate?

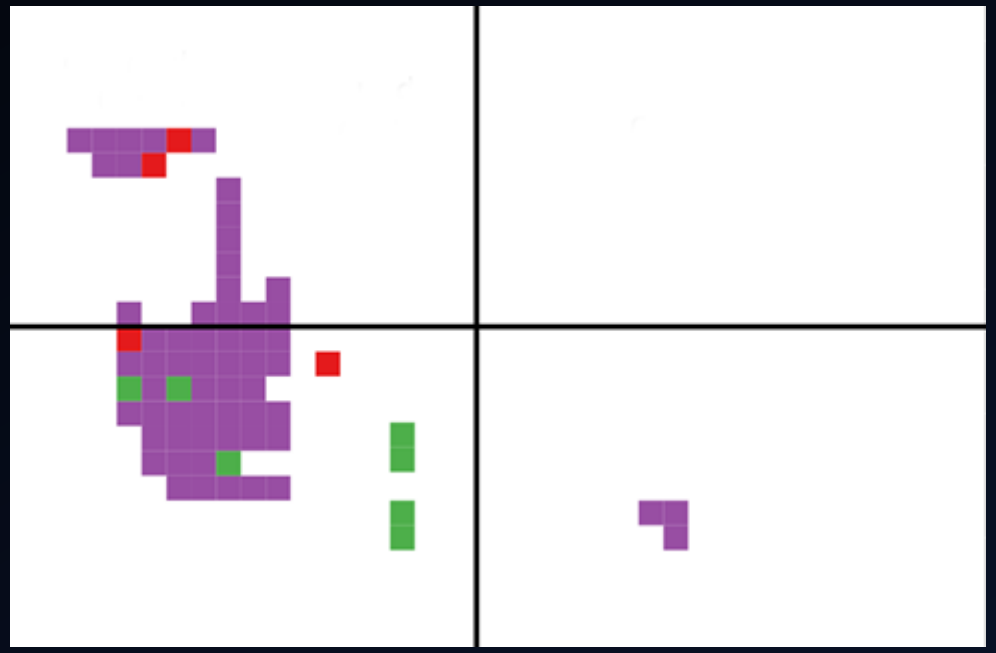


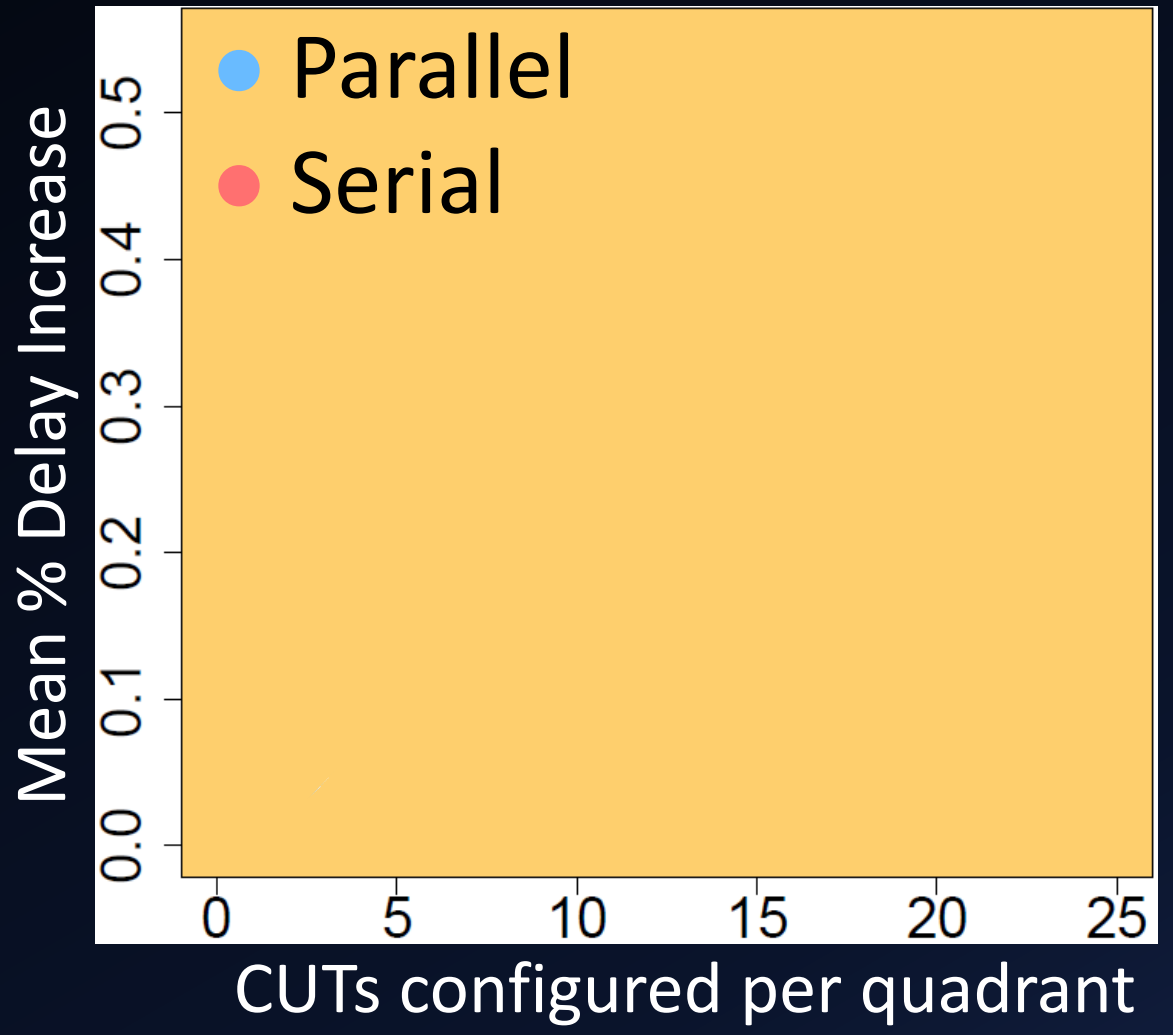
LUT-to-LUT delays



Parallelism Affects Results

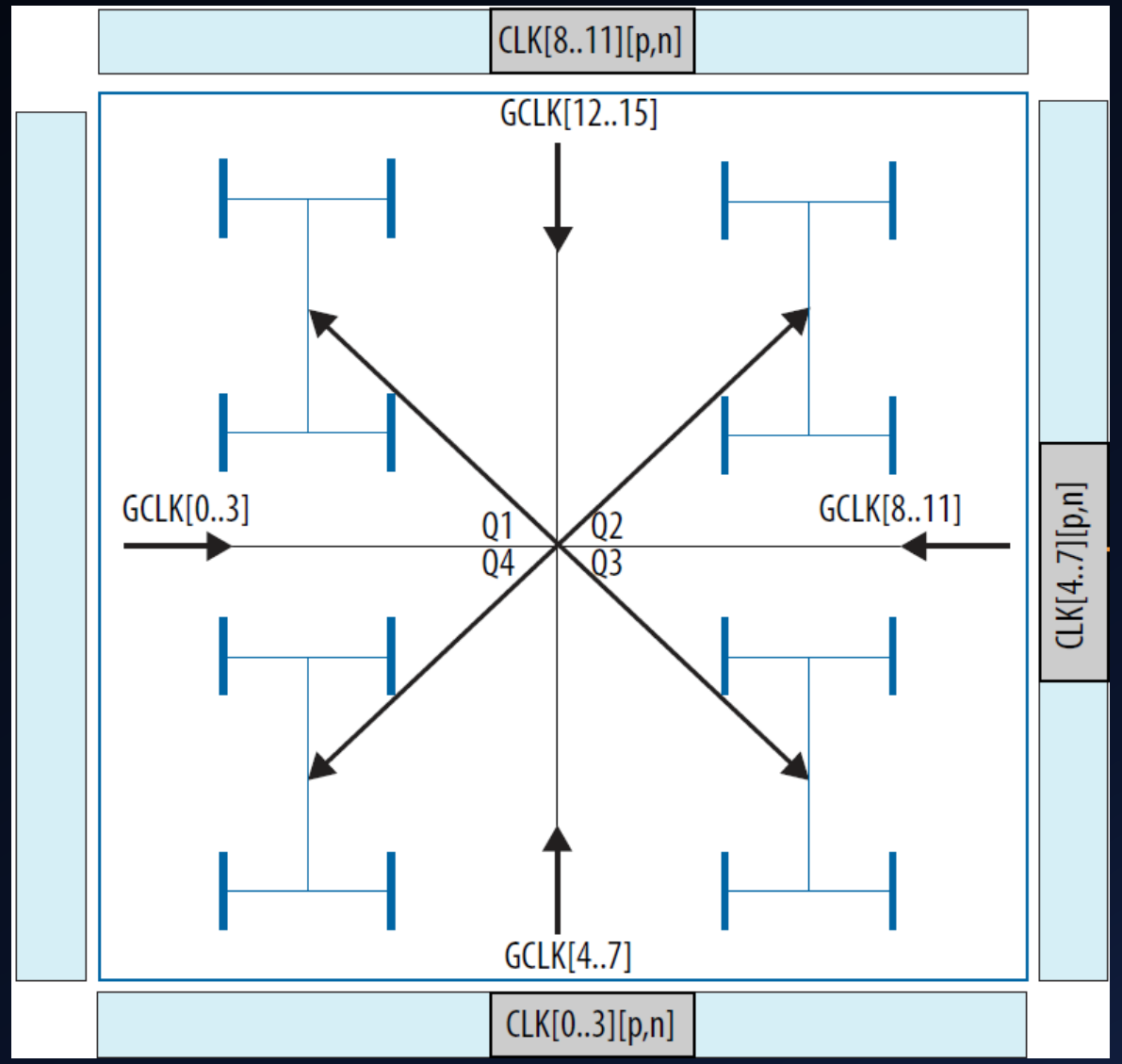
- Activating logic increases delays
- Instantiating logic increases measured delays





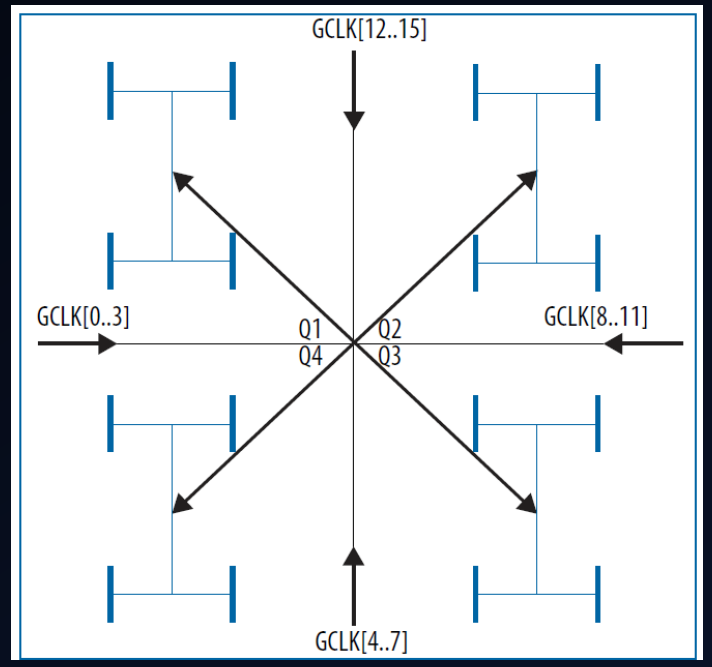
What's Happening?

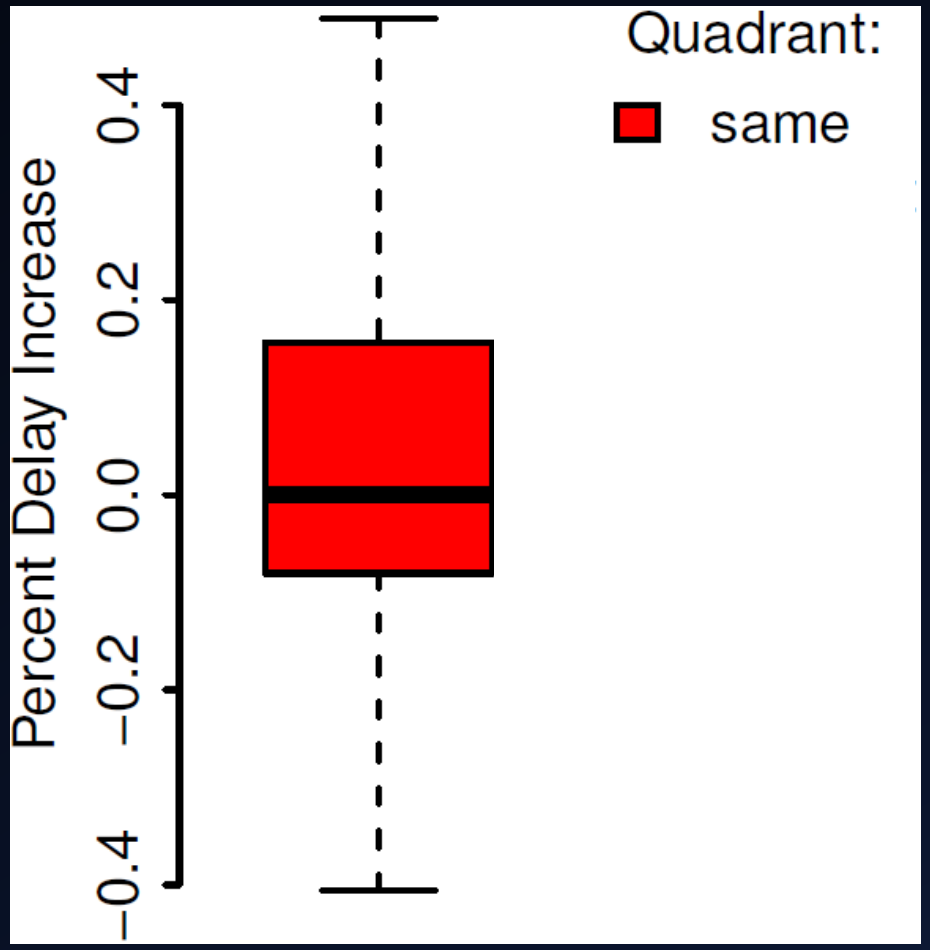
- Self-heating
- Voltage loading
- Increased clock activity
  - Placement of circuits activates additional clocks



Relative Location Affects Results

- Parallel measurement in same quadrants increases variation
- Use of different quadrants mitigates error





Conclusions

- Parallel measurement possible with increased error
- Inactive logic increases error
- Informed placement of logic improves accuracy