Conference Program of the
25th ACM/SIGDA International Symposium on
Field-Programmable Gate Arrays

February 22 - 24, 2017

Monterey Marriott Hotel, Monterey, California
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<td>9:00</td>
<td>Welcome and Opening Remarks&lt;br&gt;&lt;i&gt;John Wawrzynek (UC Berkeley)&lt;/i&gt;</td>
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<td>9:10</td>
<td>Paper Presentations (<a href="http://olaf.eecs.berkeley.edu/program">http://olaf.eecs.berkeley.edu/program</a>)</td>
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<tr>
<td>12:00</td>
<td><strong>Lunch (Ferrantes Room, 10th Floor)</strong></td>
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<td>1:30</td>
<td>Deep Learning -- Tutorial and Recent Trends&lt;br&gt;&lt;i&gt;Song Han (Stanford and DeePhi)&lt;/i&gt;</td>
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<td>2:30</td>
<td><strong>Can FPGAs Beat GPUs in Accelerating Next-Generation Deep Neural Networks?</strong>&lt;br&gt;&lt;i&gt;Eriko Nurvitadhi, Ganesh Venkatesh, Jaewoong Sim, Debbie Marr, Randy Huang, Jason Gee Hock Ong, Yeong Tat Liew, Srivatsan Krishnan, Duncan Moss, Suchit Subhaschandra, Guy Boudoukh, Intel&lt;/i&gt;</td>
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<tr>
<td>3:00</td>
<td>Break</td>
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<tr>
<td>3:30</td>
<td><strong>Accelerating Binarized Convolutional Neural Networks with Software-Programmable FPGAs</strong>&lt;br&gt;&lt;i&gt;Ritchie Zhao&lt;sup&gt;1&lt;/sup&gt;, Weinan Song&lt;sup&gt;1&lt;/sup&gt;, Wentao Zhang&lt;sup&gt;1&lt;/sup&gt;, Tianwei Xing&lt;sup&gt;2&lt;/sup&gt;, Jeng-Hau Lin&lt;sup&gt;3&lt;/sup&gt;, Mani Srivastava&lt;sup&gt;2&lt;/sup&gt;, Rajesh Gupta&lt;sup&gt;3&lt;/sup&gt;, Zhiru Zhang&lt;sup&gt;1&lt;/sup&gt;&lt;/i&gt;&lt;br&gt;&lt;sup&gt;1&lt;/sup&gt;Cornell University, &lt;sup&gt;2&lt;/sup&gt;UCLA, &lt;sup&gt;3&lt;/sup&gt;UCSD</td>
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<tr>
<td>3:55</td>
<td><strong>Improving the Performance of OpenCL-based FPGA Accelerator for Convolutional Neural Network</strong>&lt;br&gt;&lt;i&gt;Jialiang Zhang and Jing Li, UW-Madison&lt;/i&gt;</td>
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<td>4:20</td>
<td><strong>Frequency Domain Acceleration of Convolutional Neural Networks on CPU-FPGA Shared Memory System</strong>&lt;br&gt;&lt;i&gt;Chi Zhang and Viktor Prasanna, USC&lt;/i&gt;</td>
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<td>4:45</td>
<td><strong>Optimizing Loop Operation and Dataflow in FPGA Acceleration of Deep Convolutional Neural Networks</strong>&lt;br&gt;&lt;i&gt;Yufei Ma, Yu Cao, Sarma Vrudhula, Jae-sun Seo, Arizona State University&lt;/i&gt;</td>
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<td>7:00</td>
<td><strong>Opening Reception (Ferrantes Room, 10th Floor)</strong></td>
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<tr>
<td>8:00</td>
<td>Continental Breakfast</td>
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<td>8:45</td>
<td>Welcome and Opening Remarks</td>
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<td>9:00</td>
<td>Machine Learning</td>
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<td></td>
<td><strong>An OpenCL Deep Learning Accelerator on Arria 10</strong></td>
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<tr>
<td></td>
<td><strong>FINN: A Framework for Fast, Scalable Binarized Neural Network Inference</strong></td>
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<td><strong>ESE: Efficient Speech Recognition Engine with Compressed LSTM on FPGA</strong></td>
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<td>10:15</td>
<td>Poster Session 1 and Break (San Carlos 1)</td>
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<td>11:15</td>
<td>Interconnect and Routing</td>
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<td><strong>Quality-Time Tradeoffs in Component-Specific Mapping</strong></td>
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<td><strong>Synchronization Constraints for Interconnect Synthesis</strong></td>
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<td><strong>Corolla: GPU-Accelerated FPGA Routing Based on Subgraph Dynamic Expansion</strong></td>
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<td>12:30</td>
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<td>2:00</td>
<td>Architecture</td>
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<td><strong>Don’t Forget the Memory: Automatic Block RAM Modelling, Optimization, and Architecture Exploration</strong></td>
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<td><strong>Automatic Construction of Program-Optimized FPGA Memory Networks</strong></td>
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*Xilinx and Norwegian University of Science and Technology, Xilinx and University of Sydney, Xilinx, University of Sydney, Norwegian University of Science and Technology*
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<td>2:50</td>
<td><strong>NAND-NOR: A Compact, Fast, and Delay Balanced FPGA Logic Element</strong></td>
<td>Zhihong Huang, Xing Wei, Grace Zgheib, Wei Li, Yu Lin, Zhenghong Jiang, Kaihui Tu, Paolo Ienne, Haigang Yang</td>
<td>1Chinese Academy of Sciences, 2EPFL</td>
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<td>2:55</td>
<td><strong>120-core microAptiv MIPS Overlay for the Terasic DE5-NET FPGA board</strong></td>
<td>Nachiket Kapre, Prashanth Ravi, Gourav Modi, Chethan Kumar H B</td>
<td>1University of Waterloo, 2Nanyang Technological University, 3NTU</td>
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<td>3:00</td>
<td><strong>Poster Session 2 and Break (San Carlos 1)</strong></td>
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**CAD Tools**  
Chair: Lesley Shannon, Simon Fraser University

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<td>4:00</td>
<td><strong>A Parallelized Iterative Improvement Approach to Area Optimization for LUT-Based Technology Mapping</strong></td>
<td>Gai Liu and Zhiru Zhang</td>
<td>Cornell University</td>
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<td>4:25</td>
<td><strong>A Parallel Bandit-Based Approach for Autotuning FPGA Compilation</strong></td>
<td>Chang Xu, Gai Liu, Ritchie Zhao, Stephen Yang, Guojie Luo, Zhiru Zhang</td>
<td>1Peking University, 2Cornell University, 3Xilinx</td>
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<td>6:30</td>
<td><strong>Banquet (San Carlos 2-4)</strong></td>
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<td>7:45</td>
<td><strong>Banquet Panel: FPGAs in the Cloud</strong></td>
<td>Chair: George Constantinides, Imperial College London</td>
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<td>Panelists: Andrew Putnam (Microsoft, USA), Wei Qi (Baidu, China), Gaurav Singh (Xilinx, USA), Mark Shand (Waymo, USA), Ling Shao (IBM Research, China), Richard Veitch (Maxeler, USA)</td>
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**Friday February 24 (All Technical Sessions in San Carlos 2-4)**

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<td>8:00</td>
<td><strong>Continental Breakfast</strong></td>
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<td>9:00</td>
<td><strong>High-Level Synthesis -- Tools and Applications</strong></td>
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<td>Chair: Stephen Neuendorffer, Xilinx</td>
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<td>9:00</td>
<td><strong>Hardware Synthesis of Weakly Consistent C Concurrency</strong></td>
<td>Nadesh Ramanathan, Shane Fleming, John Wickerson, George Constantinides</td>
<td>Imperial College London</td>
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<td>9:25</td>
<td><strong>A New Approach to Automatic Memory Banking using Trace-Based Address Mining</strong></td>
<td>Yuan Zhou, Khalid Al-Hawaj, Zhiru Zhang</td>
<td>Cornell University</td>
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<td>9:50</td>
<td><strong>Dynamic Hazard Resolution for Pipelining Irregular Loops in High-Level Synthesis</strong></td>
<td>Steve Dai, Ritchie Zhao, Gai Liu, Shreesha Srinath, Udit Gupta, Christopher Batten, Zhiru Zhang</td>
<td>1Cornell University, 2Harvard University</td>
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### 9:55 Accelerating Face Detection on Programmable SoC Using C-Based Synthesis

**Nitish Srivastava**, **Steve Dai**, **Rajit Manohar**, **Zhiru Zhang**  
1Cornell University, 2Cornell NYC Tech

### 10:00 Packet Matching on FPGAs Using HMC Memory: Towards One Million Rules

University of Toronto

## 10:05 Poster Session 3 and Break (San Carlos 1)

## Graph Processing Applications

Chair: Nachiket Kapre, University of Waterloo

### 11:00 Boosting the Performance of FPGA-based Graph Processor using Hybrid using Hybrid Memory Cube: A Case for Breadth First Search

**Jialiang Zhang**, **Soroosh Khoram**, **Jing Li**, UW-Madison

### 11:25 ForeGraph: Exploring Large-scale Graph Processing on Multi-FPGA Architecture

**Guohao Dai**, **Tianhao Huang**, **Yuze Chi**, **Ningyi Xu**, **Yu Wang**, **Huazhong Yang**  
1Tsinghua University, 2UCLA, 3Microsoft Research Asia

### 11:50 FPGA-Accelerated Transactional Execution of Graph Workloads

**Xiaoyu Ma**, **Dan Zhang**, **Derek Chiou**  
1UT-Austin, 2University of Texas at Austin, 3Microsoft/UT Austin

## 12:15 Lunch (Ferrantes Room, 10th Floor)

## Virtualization and Applications

Chair: John Lockwood, Algo-Logic Systems

### 2:00 Enabling Flexible Network FPGA Clusters in a Heterogenous Cloud Data Center

**Naif Tarafdar**, **Thomas Lin**, **Eric Fukuda**, **Hadi Bannazadeh**, **Alberto Leon-Garcia**, **Paul Chow**, University of Toronto

### 2:25 Energy Efficient Scientific Computing on FPGAs using OpenCL

**Dennis Weller**, **Fabian Oboril**, **Dimitar Lukarski**, **Juergen Becker**, **Mehdi Tahoori**  
1Karlsruhe Institute of Technology, 2PARALUTION Labs

### 2:50 Secure Function Evaluation using an FPGA Overlay Architecture

**Xin Fang**, **Stratis Ioannidis**, **Miriam Leeser**, Northeastern University

## 3:15 Break
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<td>FPGA Acceleration for Computational Glass-Free Displays</td>
<td>Zhuolun He and Guojie Luo, Peking University</td>
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<td>4:10</td>
<td>Hardware Acceleration of the Pair-HMM Algorithm for DNA Variant Calling</td>
<td>Sitao Huang¹, Gowthami Jayashri Manikandan², Anand Ramachandran², Kyle Rupnow³, Wen-mei W. Hwu², Deming Chen²</td>
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<td></td>
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<td>¹University of Illinois at Urbana-Champaign, ²UIUC, ³Advanced Digital Sciences Center</td>
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<td>4:35</td>
<td>Conference Closing and Best Paper Award</td>
<td>Jason Anderson (University of Toronto), Jonathan Greene (Microsemi)</td>
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<td>Measuring the Power-Constrained Performance and Energy Gap between FPGAs and Processors</td>
<td>Andy Ye¹ and Karthik Ganesan²</td>
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<td>¹Ryerson University, ²University of Toronto</td>
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<td>A Mixed-Signal Data-Centric Reconfigurable Architecture enabled by RRAM Technology</td>
<td>Yue Zha¹, Jialiang Zhang¹, Zhiqiang Wei², Jing Li¹</td>
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<td>¹UW-Madison, ²Panasonic</td>
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<td>A Framework for Iterative Stencil Algorithm Synthesis on FPGAs from OpenCL Programming Model</td>
<td>Shuo Wang and Yun Liang, Peking University</td>
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<td>Scala Based FPGA Design Flow</td>
<td>Yanqiang Liu¹, Yao Li¹, Weilun Xiong¹, Meng Lai¹, Cheng Chen², Zhengwei Qi¹, Haibing Guan¹</td>
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<td>¹Shanghai JiaoTong University, ²Morgan Stanley</td>
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<td>Thermal Flattening in 3D FPGAs using Embedded Cooling</td>
<td>Girish Deshpande and Dinesh Bhatia, UT-Dallas</td>
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<td>A Machine Learning Framework for FPGA Placement</td>
<td>Gary Grewal, Shawki Areibi, Matthew Westrik, Ziad Abuowaimer, Betty Zhao,</td>
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<td>University of Guelph</td>
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<td>Precise Coincidence Detection on FPGAs: Three Case Studies</td>
<td>Ralf Salomon and Ralf Joost, University of Rostock</td>
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<td>DTP: Enabling Exhaustive Exploration of FPGA Temporal Partitions for Streaming HPC Applications</td>
<td>Mostafa Koraei¹, Magnus Jahre², S.Omid Fatemi¹</td>
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<td>¹Tehran University, ²Norwegian University of Science and Technology</td>
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<td>Accurate and Efficient Hyperbolic Tangent Activation Function on FPGA using the DCT Interpolation Filter</td>
<td>Ahmed Abdelsalam, Pierre Langlois, Farida Cheriet</td>
<td>École Polytechnique de Montréal</td>
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<td>An FPGA Overlay Architecture for Cost Effective Regular Expression Search</td>
<td>Thomas Luinaud, J.M. Pierre Langlois, Yvon Savaria</td>
<td>École Polytechnique de Montréal</td>
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<td>Storage-Efficient Batching for Minimizing Bandwidth of Fully-Connected Neural Network Layers</td>
<td>Yongming Shen, Michael Ferdman, Peter Milder</td>
<td>Stony Brook University</td>
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<td>Using Vivado-HLS for Structural Design: a NoC Case Study</td>
<td>Zhipeng Zhao and James C. Hoe</td>
<td>CMU</td>
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<td>Automatic Generation of Hardware Sandboxes for Trojan Mitigation in Systems on Chip</td>
<td>Christophe Bobda¹, Taylor Whitaker¹, Charles Kamhoua², Kevin Kwiat², Laurent Njilla²</td>
<td>¹University of Arkansas, ²Air Force Research Lab</td>
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<td>Accelerating Financial Market Server through Hybrid List Design</td>
<td>Haohuan Fu¹, Conghui He¹, Huabin Ruan¹, Itay Greenspon², Wayne Luk², Yongkang Zheng⁴, Junfeng Liao¹, Qing Zhang⁴, Guangwen Yang¹</td>
<td>¹Tsinghua University, ²Maxeler Technologies, ³Imperial College London, ⁴China Financial Futures Exchange</td>
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<td>Joint Modulo Scheduling and Memory Partitioning with Multi-Bank Memory for High-Level Synthesis</td>
<td>Tianyi Lu, Shouyi Yin, Xianqing Yao, Zhichong Xie, Leibo Liu, Shaojun Wei</td>
<td>Tsinghua University</td>
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<td>A Batch Normalization Free Binarized Convolutional Deep Neural Network on an FPGA</td>
<td>Hiroki Nakahara¹, Haruyoshi Yonekawa¹, Hisashi Iwamoto², Masato Motomura³</td>
<td>¹Tokyo Institute of Technology, ²Poco a Poco Networks, ³Hokkaido University</td>
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<td>A 7.663-TOPS 8.2-W Energy-efficient FPGA Accelerator for Binary Convolutional Neural Networks</td>
<td>Yixing Li¹, Zichuan Liu², Kai Xu¹, Fengbo Ren¹, Hao Yu²</td>
<td>¹Arizona State University, ²Nanyang Technological University</td>
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<td>CPU-FPGA Co-Optimization for Big Data Applications: A Case Study of In-Memory Samtool Sorting</td>
<td>Jason Cong¹, Zhenman Fang¹, Muhuan Huang², Libo Wang¹, Di Wu¹</td>
<td>¹UCLA, ²University of California, Los Angeles</td>
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<td>Stochastic-Based Multi-stage Streaming Realization of a Deep Convolutional Neural Network</td>
<td>Mingjie Lin and Mohammed Alawad</td>
<td>University of Central Florida</td>
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<td>fpgaConvNet: Automated Mapping of Convolutional Neural Networks on FPGAs</td>
<td>Stylianos Venieris and Christos Bouganis</td>
<td>Imperial College London</td>
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| **FPGA-based Hardware Accelerator for Image Reconstruction in Magnetic Resonance Imaging**  
*Emanuele Pezzotti¹, Alex Iacobucci¹, Gregory Nash², Umer Cheema¹, Paolo Vinella¹, Rashid Ansari¹*  
¹University of Illinois at Chicago, ²University of Illinois at Chicago, Altera |
| **ASAP: Accelerated Short Read Alignment on Programmable Hardware**  
*Subho Banerjee, Mohamed El Hadedy, Jong Bin Lim, Daniel Chen, Zbigniew T. Kalbarczyk, Deming Chen, Ravishankar K. Iyer, UIUC* |
| **RxRE: Throughput Optimization for High-Level Synthesis using Resource-Aware Regularity Extraction**  
*Atieh Lotfi and Rajesh Gupta, UCSD* |
| **GRT 2.0: An FPGA-based SDR Platform for Cognitive Radio Networks**  
*Haoyang Wu¹, Tao Wang¹, Zhiwei Li¹, Boyan Ding¹, Xiaoguang Li¹, Tianfu Jiang¹, Jun Liu¹, Songwu Lu²*  
¹Peking University, ²UCLA |
| **FPGA Implementation of Non-Uniform DFT for Accelerating Wireless Channel Simulations**  
*Srinivas Siripurapu¹, Aman Gayasen², Nitin Chandrachoodan¹, Padmini Gopalakrishnan²*  
¹IIT Madras, ²Xilinx |
| **Learning Convolutional Neural Networks for Data-Flow Graph Mapping on Spatial Programmable Architectures**  
*Shouyi Yin, Dajiang Liu, Lifeng Sun, Xinhao Lin, Leibo Liu, Shaojun Wei*  
Tsinghua University |
| **Cache Timing Attacks from The SoC FPGA Coherency Port**  
*Sumanta Chaudhuri, Telecom ParisTech* |
| **Dynamic Partitioning for Library based Placement on Heterogeneous FPGAs**  
*Fubing Mao¹, Wei Zhang², Bingsheng He³, Siew Kei Lam¹*  
¹Nanyang Technological University, ²Hong Kong University of Science and Technology, ³National University of Singapore |
| **An Energy-Efficient Design-Time Scheduler for FPGAs Leveraging Dynamic Frequency Scaling Emulation**  
*Wei Ting Loke¹ and Chin Yang Koay²*  
¹National University of Singapore, ²Xilinx Asia Pacific |